Birla Institute of Technology and Science Pilani (Rajasthan)
Department of Electrical and Electronics Engineering
EEE/INSTR F313 Analog Digital VLSI Design

Date : 08/1/2016 **COMPREHENSIVE EXAM** **Max. Time: 3 hours**
Time: 09:00 AM to 12:00 PM **(Closed Book)** **Max.Marks:100**

General Instructions to the candidate

*Please write your answers legibly and neatly. Answer **section-A and B** in **separate** answer booklets.*
Symbols, constants, terminology used have their usual meaning unless specified specially.
*There are a total of **FIVE** questions and all are compulsory. Each carries marks as indicated.*
*Answer the **sub-parts** of a question at one place and in the order in which they appear.*
*Preferably start each question on a **fresh page** however sub parts can be written in continuation.*

***Common data**: Use the following common data if not mentioned specifically in the question*
For 0.5µm Technology node $V_{DD} = 3.3V$, $V_{Thermal} = 25.9mV$

- *Use long channel approximation and lambda based design rules unless specially mentioned.*
- *Use square law current equation unless specifically mentioned.*
- *Neglect body effect, channel length modulation if not mentioned specifically.*
- *The body of all PMOS is tied to V_{DD} while all NMOS is tied to ground unless specially mentioned.*

	V_{T0} (V)	μc_{ox} (µA/V^2)	λ (V^{-1})	C_{GD0} (fF/µm)	L_{mon} (µm)
NMOS	0.7	140	0.1	0.2	1
PMOS	-0.8	40	0.1	0.2	1

Section-A Analog Design

Question No.1

a. For the current mirror shown in **Figure.1a.** Neglect body effect, channel length modulation. Given that $\boldsymbol{V_{OUT}}$ minimum is **0.5V**, $\boldsymbol{I_{REF} = 20\mu A, I_{OUT} = 50\mu A}$. (Use common data if necessary)

i. Find the node voltages at nodes A, B and C with respect to ground.

ii. Calculate the $\boldsymbol{W/L}$ of each transistor (assume all transistors of an arm have same W/L).

iii. Calculate $\boldsymbol{R_{OUT}}$ at the output node (consider Channel length modulation).

(3+6+4)

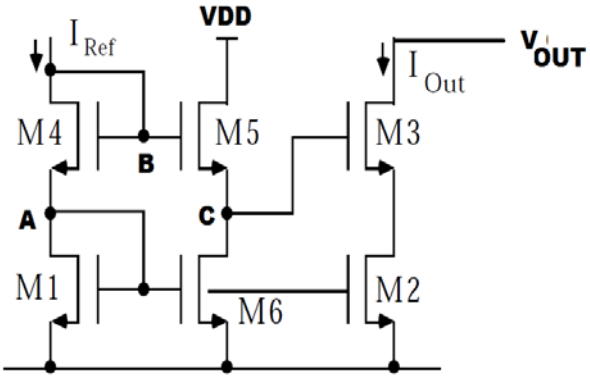


Figure-1a

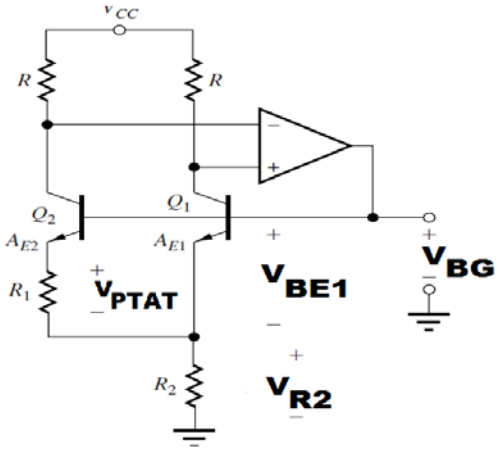


Figure -1b

b. A Voltage reference generator is shown in **Figure-1b.** Given $\boldsymbol{R = 30K\Omega}$, $\boldsymbol{R_1 = 1K\Omega}$, $\boldsymbol{R_2 = 4.16K\Omega}$ $\boldsymbol{I_{S1} = 0.1fA, A_{E2} = 10A_{E1}}$. Calculate $\boldsymbol{V_{PTAT}, V_{BE1}, I_{C1}, V_{BG}}$.

(3+3+3+3)

Question No.2

Consider the OPAMP circuit shown in Figure 2.

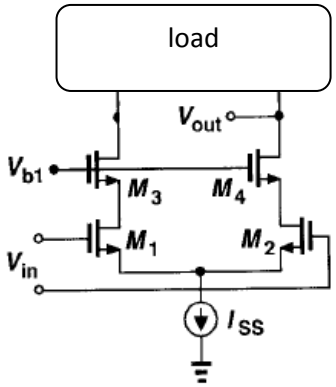


Figure. 2

(i). For Load part , Sketch and label the circuits of low voltage cascode current mirror load, conventional cascode load, conventional wilson current mirror load. The circuits should be complete.

(ii). For Iss, sketch and label a circuit of wilson current mirror (with proper modifications) with largest Rout and lowest Vomin requirement

(iii). Now sketch and label the entire circuit of Fig 1, choosing appropriate load and Iss configurations from part (a) and part (b) to get----

i. Maximum swing
ii. Maximum voltage gain (Vout/ Vin)
iii. Maximum ICMR

(21) M

Section-B Digital Design

Question No.3

(a):

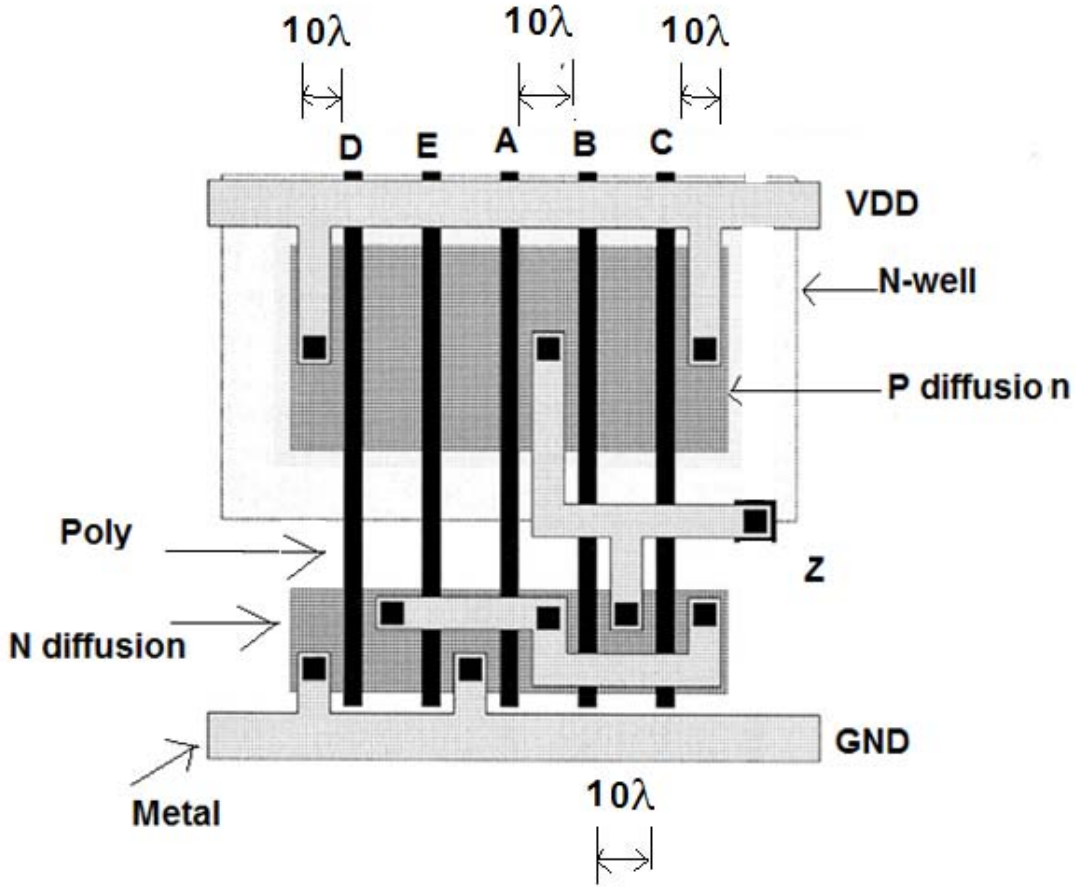


Figure 3

The layout shown in figure 3, has width i.e. W_p=40 μm, W_n=20 μm for a PMOS and NMOS transistor respectively. The length for both NMOS and PMOS transistor are equal (i.e. L_n=L_p=1 μm =2λ).

(i) Draw the equivalent transistor level circuit indicating the W/L ratios.

(ii) If $C_{j0,sw,n}$= $C_{j0,sw,\ p}$=5×10^{-10} F/m , $C_{j0,n}$= $C_{j0,\ p}$ =5×10^{-4} F/m^2, calculate the total junction capacitance at output node 'Z'.

(iii) If C_{ox}=5×10^{-3} F/m^2 then compute the gate capacitance at input node 'A'.

(Ignore the metal wire and overlap capacitances, ignore perimeter capacitance facing the poly gate)

((5+5+2) M)

(b): For an NMOS transistor with size W/L=80μm/1μm, draw the equivalent fingered layout with 8 fingers, clearly indicate width of each transistor, source, drain terminals, layers (Diff, metal, poly-silicon, contacts). Also draw the equivalent fingered schematic. **(5 M)**

Question No.4

(a) A static CMOS NOR gate uses 4 transistors, while a pseudo-nMOS NOR gate uses only 3. Unfortunately, the pseudo-nMOS output does not swing rail to rail. If both the inputs and their complements are available, it is possible to build a 3-transistors NOR that swings rail to rail without using any dynamic nodes. Show how to do it by drawing transistor level schematic. Explain any drawback of your circuit. **5M**

(b) Draw the schematic of 3-input XOR functions using each of the following circuit techniques. Note: inputs and their complements are available. **8M**

(i) Static CMOS. Use only sixteen transistors.

(ii) Dual-rail domino. Use only thirteen transistors and two inverters.

(c) Draw the schematic of 2-input NAND gate using Complementary Pass transistor logic with minimum number of transistors. Note: inputs and their complements are available. **4M**

Question No.5

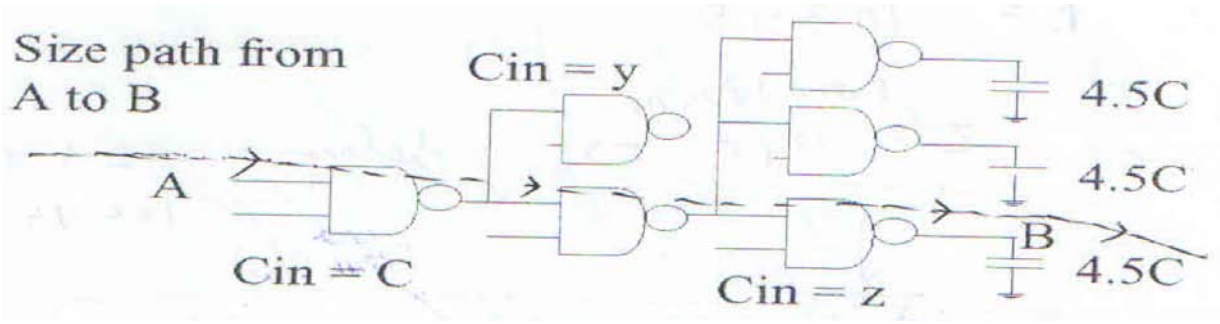
(a): For the circuit given below, all logic gates are designed to have equal worst case effective rise/fall resistance. The parameter within each symbol stands for the gate capacitance seen by one input pin. For the critical path A to B. Use: L_{min}=0.25µm, C_{ox}=20nF/µm^2

i). Use method of logical effort to find the path logical effort, electrical effort, branching effort.

ii). Now calculate the minimum delay through A to B (dashed) critical path.

iii). Next, size all the gates accordingly and annotate sizes with the PMOS and NMOS of each gate.

(6+3+3=12M)



(b) :

i). An SRAM contains 8129 8-bit words. If it is physically arranged in a square fashion, how many bits will be used in the row decode and how many bits will be used in the column decode ? (assume the cell aspect ratio is square.)

ii). A dynamic memory cell has a worst case leakage current of 2nA (independent of voltage) and is refreshed every 100µs. If the power supply is 3V and the cell voltage should not leak lower than 1.8V, find the required cell capacitance value.

(4+4=8M)

*****All The Best *****