Birla Institute of Technology and Science Pilani (Rajasthan)
Department of Electrical and Electronics Engineering
EEE/INSTR F313 Analog Digital VLSI Design

Date : 04/12/2015 **COMPREHENSIVE EXAM** **Max. Time: 3 hours**
Time: 09:00 AM to 12:00 PM **(Closed Book)** **Max.Marks:100**

General Instructions to the candidate

*Please write your answers legibly and neatly. Answer **section-A and B** in **separate** answer booklets.*
Symbols, constants, terminology used have their usual meaning unless specified specially.
*There are a total of **FIVE** questions and all are compulsory. Each carries marks as indicated.*
*Answer the **sub-parts** of a question at one place and in the order in which they appear.*
*Preferably start each question on a **fresh page** however sub parts can be written in continuation.*

***Common data**: Use the following common data if not mentioned specifically in the question*
For 0.5µm Technology node $V_{DD} = 3.3V$, $V_{Thermal} = 25.9mV$

- *Use long channel approximation and lambda based design rules unless specially mentioned.*
- *Use square law current equation unless specifically mentioned.*
- *Neglect body effect, channel length modulation if not mentioned specifically.*
- *The body of all PMOS is tied to V_{DD} while all NMOS is tied to ground unless specially mentioned.*

	V_{T0} (V)	μc_{ox} (µA/V^2)	λ (V^{-1})	C_{GD0} (fF/µm)	L_{mon} (µm)
NMOS	0.7	140	0.1	0.2	1
PMOS	-0.8	40	0.1	0.2	1

Section-A Analog Design

Question No.1

a. A Beta-Multiplier circuit shown in **Figure.1a.** is used to generate a reference voltage V_{biasn}. If the Temperature sensitive variables are Resistance R, Threshold voltage of the MOSFET and mobility. (γ=0, M3, M4 are matched and M2 is 'K' times wider than M1).

i. Derive an expression for I_{REF}. **(4)**

ii. Write an expression for reference voltage V_{biasn}. **(2)**

iii. Calculate R such that at T=300K V_{biasn} has zero temperature coefficient. Given Temperature coefficient of resistance R is $2000\ ppm/℃$, $\frac{1}{\mu_n}\frac{\partial \mu_n}{\partial T} = -\frac{1.5}{T}/℃$ (T in Kelvin), $\frac{\partial V_{THN}}{\partial T} = -0.6mV/℃$ and $(W/L)_2 = 4(W/L)_1 = 20$. **(7)**

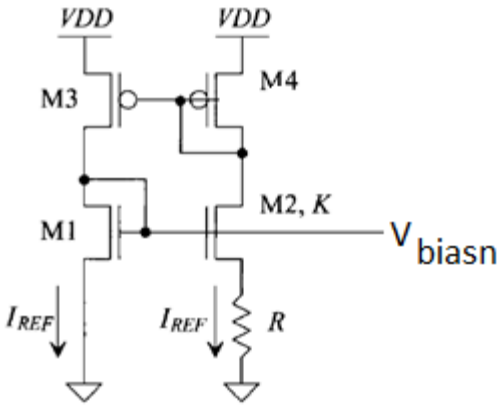

Figure-1a Question No.1a

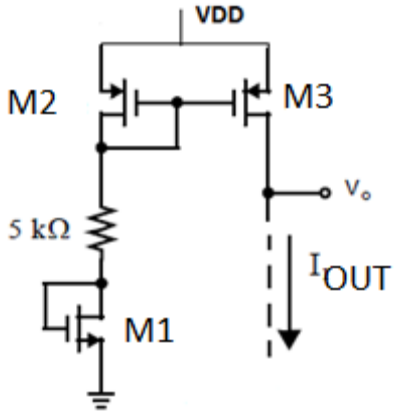

Figure -1b Question No.1b

b. Consider a current source shown in **Figure-1b.** Given all transistors have a uniform length of 1µm each and W_1=22.5 µm, W_2=78.75 µm.

i. Calculate the current through the 5kΩ resistor. **(5)**

ii. If an output current I_{OUT} of 0.5mA is desired, calculate W_3. (λ=0). **(2)**

iii. If an output current I_{OUT} of 0.5mA is desired, calculate W_3. (λ≠0). **(3)**

iv. If power-supply VDD changes by 5% then calculate the change in output current I_{OUT} using small signal equivalent. (λ=0) **(2)**

Question No.2

For circuit shown in **Figure 2a.** neglect body bias effect. Assume all transistors are operating in active region, have $V_{over-drive}$ = 0.2V and are matched pairs wherever required. I_{SS} is implemented using a basic current mirror. Do not assume all the transistors have equal g_m,r_0.

i. Write an expression for differential voltage gain vout/ vin.

ii. Write an expression for resistance at node X.

iii. Write an expression for OCMR (output common mode range).

iv. Write an expression for ICMR (input common mode range).

v. Write the value of DC voltage vb2 if all transistors have overdrive voltage of 0.2 V.

vi. Design a circuit (with transistor sizes) for generating DC voltages vb2 and vb3. Given a current I_{ref} of 50µA is available and I_{SS} = 100 µA and I(M9) =50 µA.

vii. Assuming load capacitance at node R, M, and X as C_R , C_M, and C_X, Write an expression for pole frequencies due to node R , M , and X

viii. Modify the given Op-Amp circuit of **figure 2.a**. to convert it to single ended output at node R. Now write the expression for slew rate

ix. For **figure.2.b.** Draw a circuit to fix the DC voltage to 2.3V at node V_{out2}. **(25)**

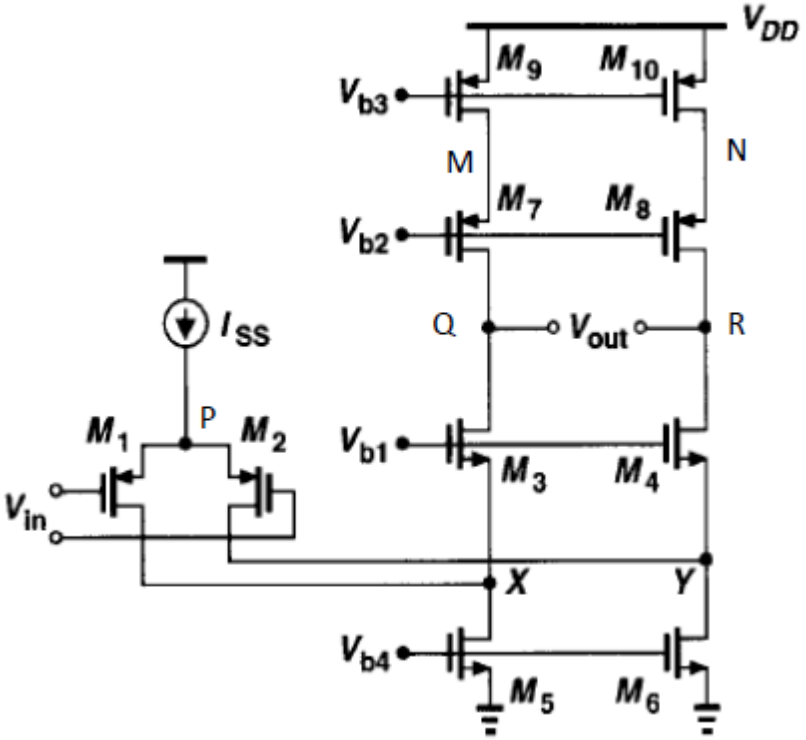

Figure 2.a. Question No.2

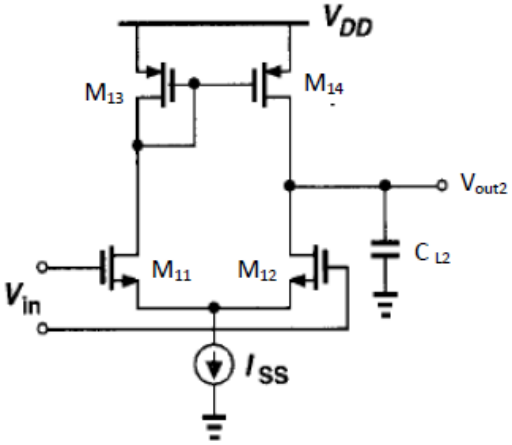

Figure 2.b. Question No.2

Section-B Digital Design

Question No.3

a. The layout shown in **Figure.3.** has equal width for both NMOS and PMOS transistor (i.e. $W_n=W_p=40\mu m$) also equal length for both NMOS and PMOS transistor (i.e. $L_n=L_p=1\ \mu m = 2\lambda$).

i. Draw the equivalent transistor level circuit indicating the W/L ratios.

ii. If $C_{j0,sw,n}= C_{j0,sw,\ p}=5\times10^{-10}$ F/m , $C_{j0,n}= C_{j0,\ p} =5\times10^{-4}$ F/m^2, calculate the total junction capacitance at output node 'Y'.

iii. If $C_{ox}=5\times10^{-3}$ F/m^2 , then compute the gate capacitance at input node 'V_A'. (Ignore the metal wire and overlap capacitances, ignore perimeter capacitance facing the poly gate)

(8)

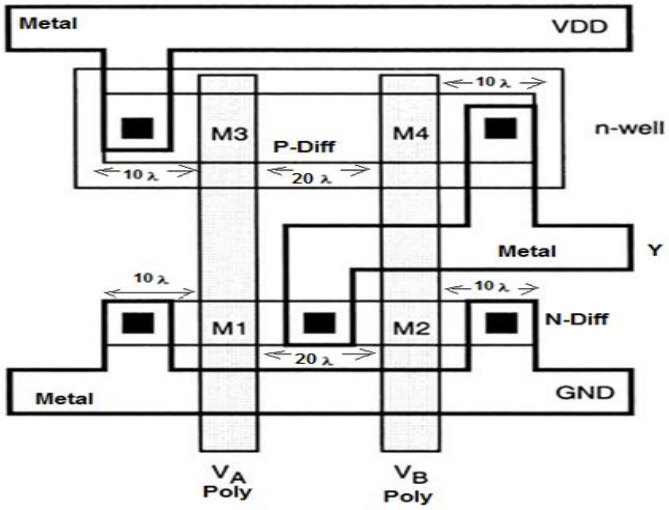

Figure.3. Question No. 3a.

b.

i. For NMOS transistor with W/L=40μm/1μm, draw the equivalent fingered layout with 4 fingers, clearly indicate width of each transistor, source, drain terminals, layers (Diff, metal, poly-silicon, contacts). Also draw the equivalent fingered schematic. **(6)**

ii. A digital circuit is fabricated in a 4μm technology and was able to operate at 100 MHz, consuming 5watts with a 2.5 V power supply. Using fixed voltage scaling, what will the speed and power consumption of the same processor be if scaled to 1 μm technology? **(3)**

Question No.4

a. Consider the Boolean function $X = ((\overline{A} + \overline{B})(\overline{C} + \overline{D} + \overline{E}) + \overline{F})\ \overline{G}$

i. Implement Boolean function (X) using static complementary CMOS.

ii. Size the transistors so that the worse case equivalent pull up and pull down resistance is the same as that of an inverter with an NMOS W/L = 2 and PMOS W/L = 6.

iii. Which input pattern(s) would give the worst and best equivalent pull-down resistance?

iv. Now, implement Boolean function ($\overline{X}$) using domino logic (n-type). **(10)**

b. Consider the circuit of **Figure.4.** Assume the inverter switches exactly at $V_{dd}/2$, neglect body effect, channel length modulation and all parasitic capacitance. Given $(W/L)_1 = (W/L)_2 = (W/L)_3 = 0.5\mu m/0.25\mu m$ and $(W/L)_4 = 1.5\mu m/0.25\mu m$

i. What is the logic function performed by this circuit at 'Out'?

ii. Explain why this circuit has non-zero static power dissipation.

iii. Modify and redraw the circuit by adding only a single transistor, so that there will not be any static power dissipation. Explain how you would choose the size of the transistor qualitatively.

iv. Implement the logic function obtained in part (i) using transmission gates only. Use minimum number of transistors. **(7)**

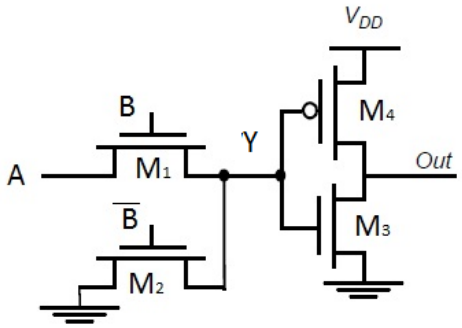

Figure.4. Question No. 4b.

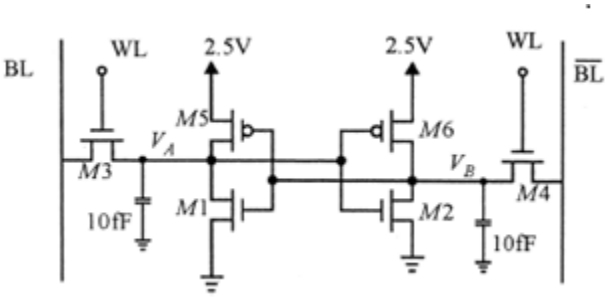

Figure.5. Question No. 5b.

Question No.5

a. Consider a bank of CMOS registers where T_{setup}= 300ps, T_{hold}= 200ps, T_{ccq}=100ps $T_{cd\ (contamination)}$ =250ps. Also assume an average gate delay equals T_{gate} = 50ps.

i. If it is desired to run a system clock at 800MHz, how many gate delays can be in the combinational logic block between registers? **(3)**

ii. If an internal delay of 50ps is inserted into every register right at the clock input, what is the new T_{setup}, T_{hold}, T_{ccq}, T_{cd}? **(3)**

b. Consider an SRAM cell as shown in the **Figure.5**, where BL and BL' are both pre-charged to V_{DD}=2.5V during a read operation. Assume: W_1 = 1.0 µm, W_3= 0.5 µm, W_5 =0.5 µm, L=0.25 µm, C_{ox}= 6fF/µm^2, $\mu_n C_{ox}$ = 120µA/V^2, $\mu_p C_{ox}$ = 30µA/V^2 and V_{TN} = -V_{TP}= 0.4V.

i. For the given parameters, calculate the peak voltage at VA during a read operation when the cell stores a "one" at VB. **(5)**

ii. Assuming this SRAM cell is one of 512X 512 array, estimate the word line capacitance for a single row. Ignore any wiring capacitance. **(5)**

*****All The Best *****