Birla Institute of Technology and Science Pilani (Rajasthan)
Department of Electronics and Electrical Engineering
Analog Digital VLSI Design (EEE/INSTR F313)
First Semester 2015-16

Date : 06/10/2015 **MID TERM EXAM** **Max. Time: 30 minutes**
Time: 02:00 to 03:30 PM **(Part-A Closed Book)** **Max.Marks:30**

Name_____ **ID No.** | | | | | | | | | | | | | |

Instructions to the candidate

*Please write your answers legibly and neatly in the **space provided** only.*
Cuttings / Overwriting will make a question invalid.
*There is no **partial marking** in this section of the exam.*
Symbols, constants used have their usual meaning unless specified specially.
*There are a total of **FIFTEEN** questions and all are compulsory.*
You may use the supplementary answer sheet for rough work which will not be considered for evaluation.

***Common data for PART-A**: Use the following data if not mentioned specifically in the question.*
$V_{DD} = 3V$, $|V_{T0P}| = 0.8V, V_{T0N} = 0.6V$, $KP_P = 20\ \mu A/V^2, KP_N = 60\mu A/V^2$, $C_L = 100fF$, $f = 850MHz$, $Lmin\ (2\lambda) = 0.3\mu m$.
Use long channel approximation and lambda based design rules unless specially mentioned.
The body of all PMOS is tied to V_{DD} while all NMOS is tied to ground.
Use Square Law relation for PMOS as well as NMOS.

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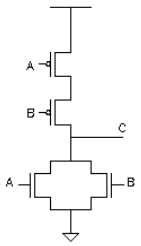
*Question No. 1-8 each carries **THREE** marks.*

1. Calculate the aspect ratio (W/L) of PMOS that has to source a maximum current of 300 μA.

Ans. _____

2. A 2 input NOR gate is implemented in static CMOS style. The reference inverter is designed for $T_{PHL}=T_{PLH}$ case and $W_N=2L_{min}$. Calculate the width of all the MOSFETS in µm.



Ans. W_{pA}_____ W_{pB}_____
Ans. W_{nA}_____ W_{nB}_____

3. A 3 stage path has a path effort of F=850. then find the delay(in ps) of this path using optimal number of stages obtained using logic effort model (given $P_{inv}=1$, FO4 delay = 60ps).

Ans. _____

4. Draw the schematic and properly label all the signals of a simple 1 transistor DRAM cell.

5. For the circuit shown below (fig.1) what is the maximum permissible positive clock skew.

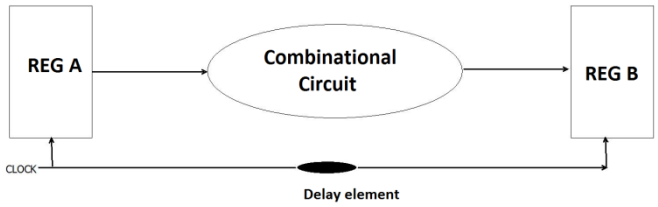


Figure 1: Question no.5

$T_{cd\text{-}Logic} = 30$ ps
$T_{p\text{-}cq\text{-}A} = 25$ps
$T_{cd\text{-}cq\text{-}A} = 15$ps
$T_{su\text{-}A} = 45$ps
$T_{hold\text{-}A} = 25$ps
$T_{p\text{-}cq\text{-}B} = 25$ ps
$T_{cd\text{-}cq\text{-}B} = 20$ ps
$T_{su\text{-}B} = 30$ ps
$T_{hold\text{-}B} = 35$ ps
$T_{pd\text{-}Logic} = 125$ ps

Ans. _____

6. Sketch a positive latch using Truly Single Phase Clock (TSPC).

7. In a certain scaling strategy the scaling factor for Voltage is chosen as 0.8 while all the geometrical dimensions are scaled by 0.6. Calculate the scaling factor of power (static) density.

Ans. _____

8. A 2 input NAND gate is implemented in static CMOS style if P(A=1)= P(B=1)=0.5 calculate the dynamic power consumption in mW at the output node.

Ans. _____

*Question No. 9-15 each carries **ONE** mark.*

9. Circuit used to detect a very small change of voltage on bit lines is called _____

10. _____ gate can't be implemented in Pass Transistor Logic.

11. The _____ layout strategy is used for boundary matching.

12. Large ingots of Single crystal silicon are grown mostly using _____ process.

13. _____ process is used to transfer patterns to each layer of IC.

14. The interconnection between two different metal layers is provided through _____.

15. **A:** Drain/Source diffusion **B:**Gate oxide formation **C:**Poly for gate material

Arrange the following unit step processes in the correct sequence as they are performed to form a CMOS in a N-well process. _____.

*****All The Best******

(Part-B Open Book)

General Instructions to the candidate

Please write your answers legibly and neatly in the answer booklet provided only.
Symbols, constants, terminology used have their usual meaning unless specified specially.
*There are a total of **FIVE** questions and all are compulsory. Each carries marks as indicated.*
*Answer the **subparts** of a question at one place and in the order in which they appear.*
*Preferably start each question on a **fresh page** however sub parts can be written on same side.*

***Common data**: Use the following common data if not mentioned specifically in the question*
For 0.5µm Technology node $V_{DD} = 3.3V$, $V_{Thermal} = 25.9mV$

- *Use long channel approximation and lambda based design rules unless specially mentioned.*
- *Use square law current equation unless specifically mentioned.*
- *Neglect body effect, channel length modulation if not mentioned specifically.*
- *The body of all PMOS is tied to V_{DD} while all NMOS is tied to ground unless specially mentioned.*

	V_{T0} (V)	K_P (µA/V^2)	λ (V^{-1})	C_{GD0} (fF/µm)	L_{mon} (µm)
NMOS	0.7	140	0.1	0.2	1
PMOS	-0.8	40	0.1	0.2	1

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[1] If a CMOS inverter circuit drives a total output load capacitance of 5 pF then

[a] Determine the channel width of the n-MOS and p-MOS transistors such that the switching threshold voltage is 1.55 V and output rise time is 4.2 nS (0 to 90% of V_{DD}).Solve using differential equation at the output node.

[b] Determine the probability of input being logic '1' if total dynamic power consumption at 100 MHz frequency is 1.30 mW. **[8+4]**

[2] For a CMOS inverter circuit $|V_{T0,n}|=|V_{T0,p}|=0.7V$, $(W/L)_n=2$, $(W/L)_p=7$. Calculate the noise margin high (NMH) and the noise margin high (NML) for the inverter. **[5]**

[3] **[a]** Draw the transistor level implementation for the given Boolean expression using pass transistor logic (you can assume complementary inputs are available and single static CMOS inverter is also available)

$$\boldsymbol{F = \overline{A} + \overline{B} + \overline{C}}$$

[b] Assume that output F drives a large load C_L =10fF, now derive an approximate expression for the worst case propagation delay of the whole circuit. Assume unit sized transistors with $R_{eqN}= R_{eqP}$ =20kΩ, $C_{intermediate\text{-}node}$=2fF.

[c] Discuss the sources of power dissipation in the circuit.

[d] If you have identified the source of power dissipation in the drawn circuit then propose at least one modification to improve the performance and power dissipation of the circuit.

[e] In order to reduce power consumption designer scales down the power supply voltage. Now, determine the minimum supply voltage for which the circuit should be operational.

[f] If the threshold voltage of this process is lowered then can you think of its impact on the power consumption and performance of the circuit.

[5+3+3+2+2+2=17M]

[4] For CMOS layout shown in Figure 1, C_{ox} = 5 x 10^{-3} F/m^2, C_{j0sw} = 5 x 10^{-10} F/m, C_{j0} = 5 x 10^{-4}

F/m^2, C_{metal1} = 0.3 x 10^{-10} F/m, Different dimensions a = 4µm, b = 5 µm, c = 1 µm, d = 6 µm, e = 2 µm, f = 20 µm, g = 15 µm and X_j (junction depth) = 1 µm. Neglect poly wiring and overlap capacitances.

[a] Draw the transistor level schematic of given layout. Label (W/L) of transistors also.

[b] Compute the capacitance at node A and node B. **[4+4]**

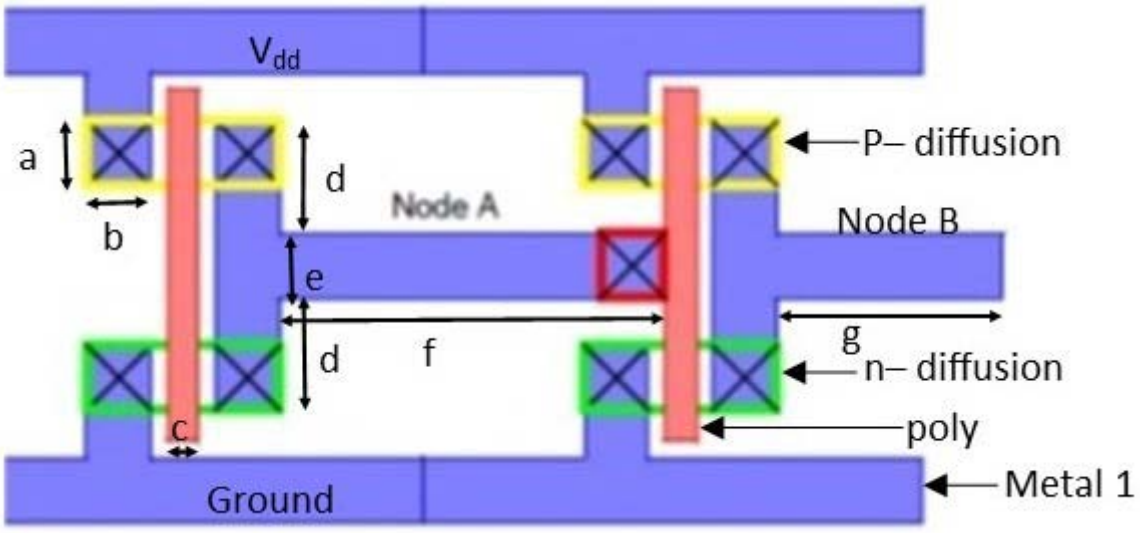

Figure 2: Question No.4

[5] A 10x unit-sized inverter drives a 2x inverter at the end of 5mm long, 0.32 µm wide metal2 wire in 180nm process. For wire, the sheet resistance is 0.05 Ω/ and the capacitance is 0.2 fF/ µm. For unit inverter, the effective resistance is 6.9 KΩ and gate capacitance is 2fF. Compute the propagation delay using the Elmore delay model, when wire is represented with a single segment π-model. Neglect diffusion capacitances. **[8]**

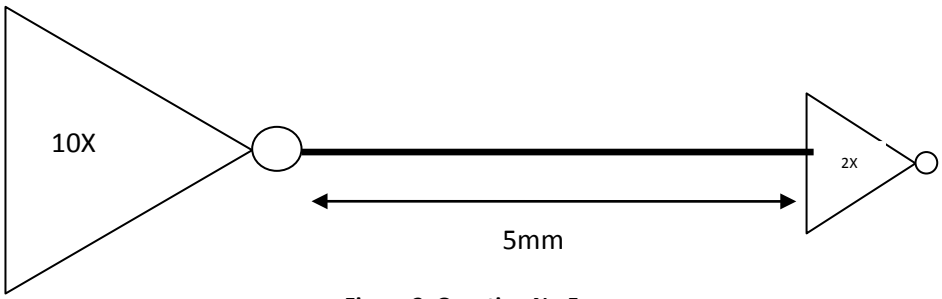

Figure 2. Question No.5

*****All The Best *****