BIRLA INSTITUTE OF TECHNOLOGY AND SCIENCE, PILANI, RAJASTHAN
I SEMESTER, 2015-2016
COMPREHENSIVE EXAMINATION
CLOSED BOOK (11 December. 2015) AN
MEL G623 ADVANCED VLSI DESIGN

TIME-3 hrs. **MAX. MARKS=35**

NOTE: state your assumptions clearly

Answers should be clear, concise and legible. Specify your assumptions clearly. Do all parts of same question together. Diagrams should be neat and labeled properly.

NO MARKS for unnecessary theoretical explanation.

Although your answers are important, your REASONS for giving those answers are even more important. Please, explain what you are doing and why. So, ***justify your answers*** Take $u_n=2u_p$

Q1.(a)A multiplexer has a maximum input capacitance of 16 units on each input. It must drive a load of 160 units. Estimate the delay of the NAND and compound gate designs

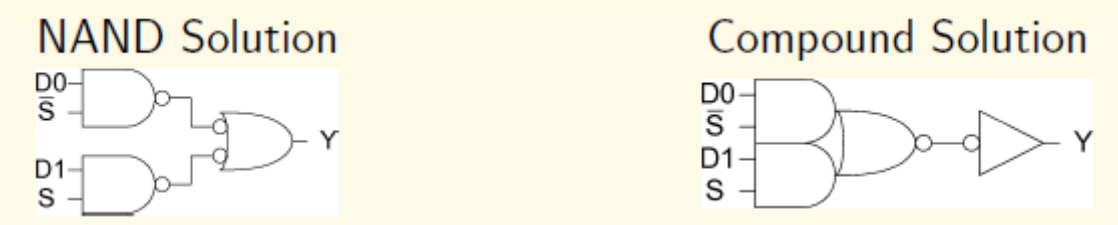

Fig 1a

4

Q1(b) Find the logical efforts for the inputs, a and c in the circuit of fig 1b for both rising and falling output. Suggest a way to reduce the parasitic delay of this circuit by modifying the structure (but keeping the same function).

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Q1(c) Suppose in fig 1c, input A of a NAND gate is most critical Using smaller transistor on A (less capacitance) and boost size of noncritical input (to get logical effort 1 approx for critical input) so that total pull down path resistance remains same. Now, calculate logical effort of input A and B`

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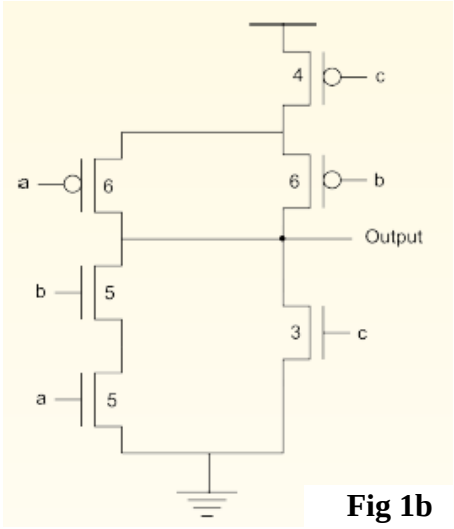

Fig 1b

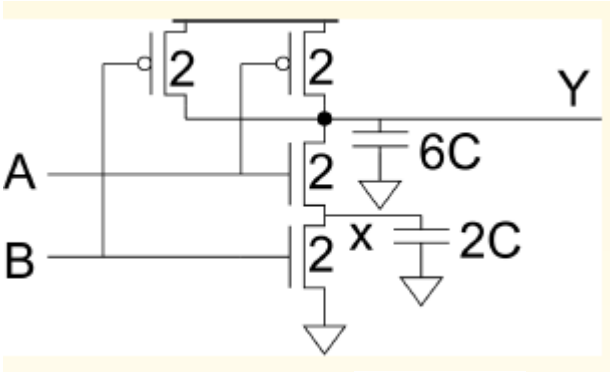

Fig 1c

Q2.For the fig. 2

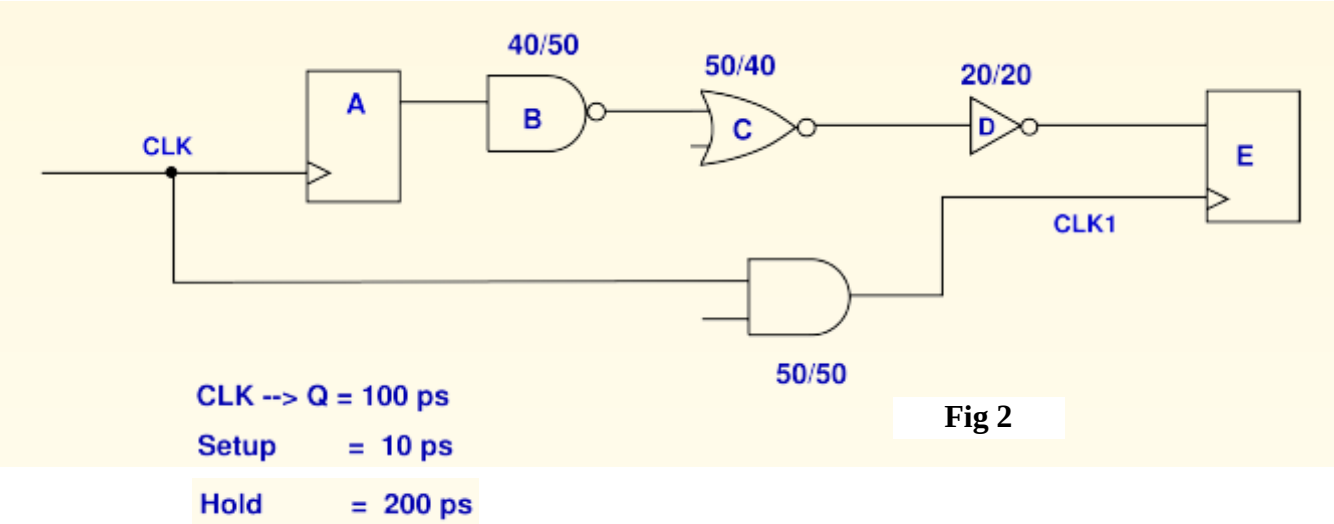

Fig 2

a. Calculate Shortest path delay from A to E
b. Determine if there is a hold time violation. If yes calculate hold slack
c. Modify the circuit to fix hold time violations. Hence determine the minimum cycle time at which the path can operate

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Q3.For the fig 3, convert it to radix 4 parallel prefix adder. Then compute its parameters l, f, t

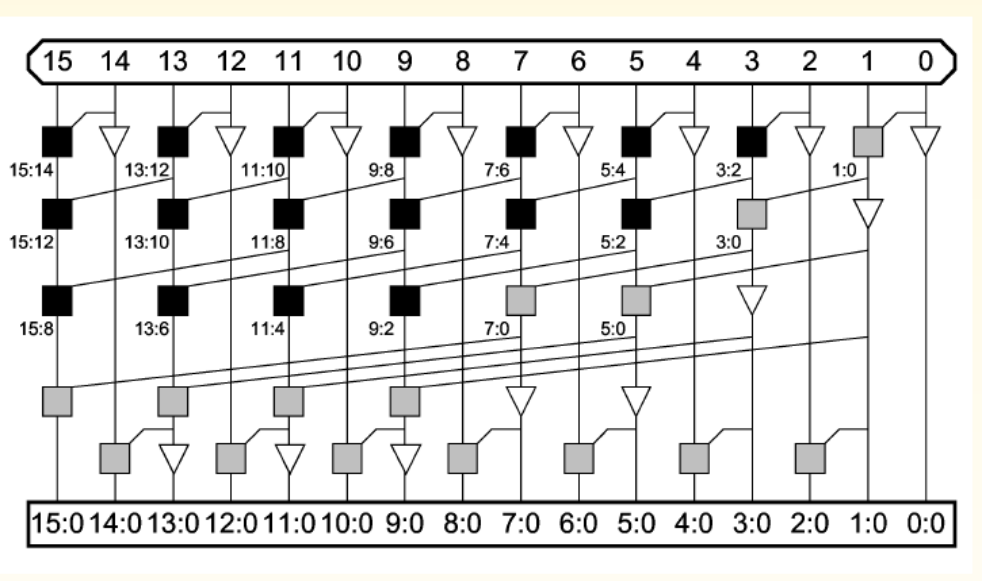

Fig 3

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Q4.For the fig 4,

a) Draw the schematics of full swing ,FS, and reduced swing , RS, buffer circuits using Vdd=3.3V. you may choose your own RS topology.
b) The conductor widths are progressively tapered in an H-tree as we move away from the clock source. Explain the reason for it

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c) Considering transmission line effects, with characteristic impedance (Z_0) as 50 ohms, $Z_{Source} = 5 Z_0$, $\mathbf{Z}_T=\infty$ for wire length of 4ns between any two FS buffers in given H network, draw lattice diagram to find the time for signal to reach destination

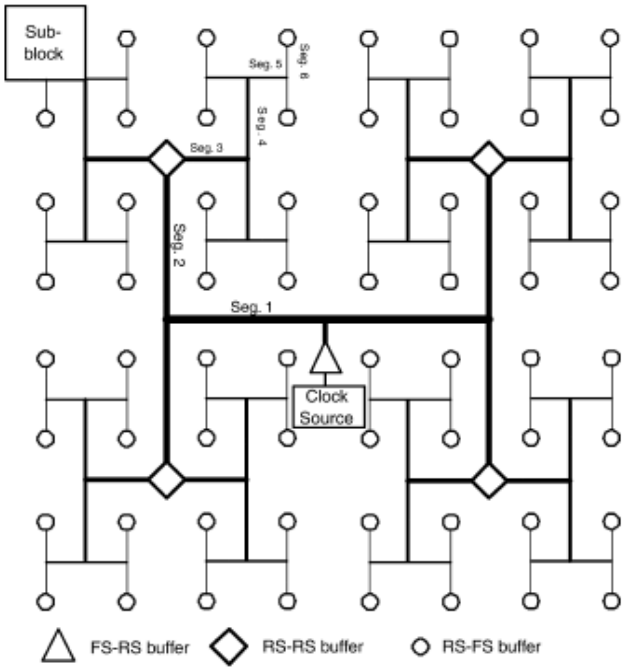

Fig 4

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Q5.(a) For synchronizer circuit of fig 5, describe the operation. What is the purpose of clkL, clkE , donewaiting signals?

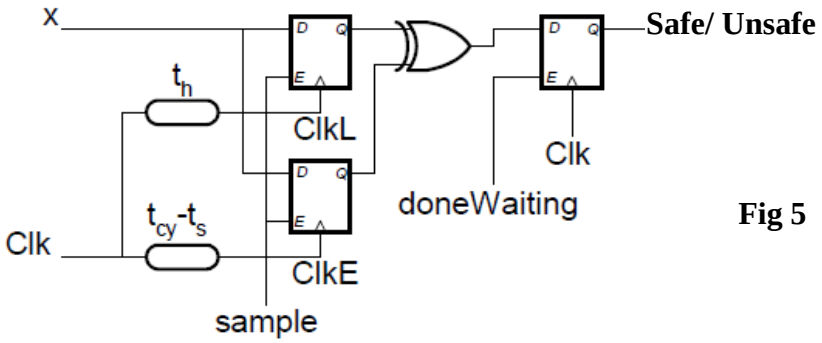

Fig 5

(b) metastability of flip flop is governed by equation--

$$P_2(\text{metastable}) = P_2(\text{enter metastability}) \times P_2(\text{still in state after } t_R)$$

Modify above equation for 2 flop synchronizer. Hence write modified equation of MTBF (mean time between failure) for 2 flop synchronizer..

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