Birla Institute of Technology & Science
I[st] Semester 2015-16
MEL G626 VLSI Test and Testability
Test 2 (Open Book)

MM:20 **Duration: 50 Min** **Date: 04/11/2015**

Q1: What are the advantages of scripting language? **(2 M)**

Q2: Print the output of following system verilog program? **(3 M)**

```
program main();
int a;
initial
begin
a = 5
#10 a = 10;
#10 a = 20;
#10 a = 30;
#10 $finish;
end
```

```
task pass_xyz(int i);
forever @i
$display("pass_xyz: I is %0d",i);
endtask
initial
pass_xyz(a);
endprogram
```

Q3: Write a system verilog program using a function which takes an array of 2-state, 32-bit unsigned integer consisting of elements 2,4,8,16,32,64,128 as input and returns the result as ANDED operation of these values and displays result. Also write its output. **(4M)**

Q4: Indentify the error if any in the following system verilog codes? If yes then correct the error or else write the output, justify your answers. **(4M)**

code1:

```
class A ;
static int i;
endclass

program main ;
A x;
initial
begin
x.i = 123;
$display(x.i);
end
```

code2:

```
class B ;
int j;
virtual static task incr();
$display("J is %d",j);
endtask
endclass
```

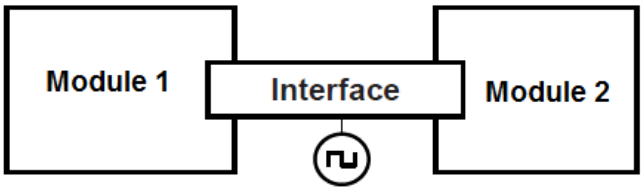
code3:

```
class C ;
const int x;

function new();
ix= 20;
x++;
endfunction
endclass
```

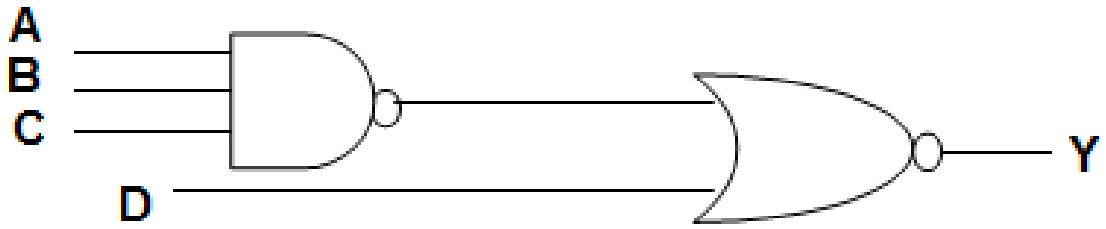
Q5: The module1 and module2 are sharing a common interface which has common input clock 'clk' which is externally fed to interface. Also the other common signal present in both the modules are 2-bit 'p', 2-bit 'q'

and 1-bit 'r'. Write an interface 'xyz_inf' and top module which is described using this interface and these two modules. **(3M)**



Q6: For the circuit shown below, (i) mark all faults (ii) remove faults using equivalent collapsing and compute the collapse ratio. (iii) remove faults using dominance collapsing and compute the collapse ratio.

(4 M)



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