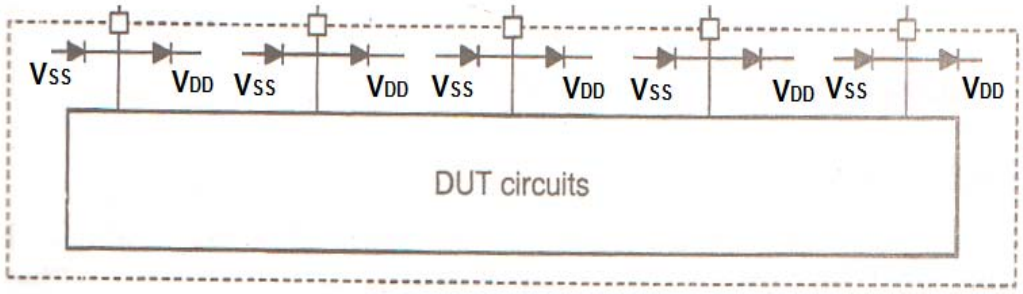
Birla Institute of Technology & Science
I[st] Semester 2015-16
MEL G626 VLSI Test and Testability
Test 1 (Closed Book)

MM:20 **Duration: 50 Min** **Date: 28/09/2015**

Q1: Answer the following questions in brief:
(i) List the several power mode verification in a SOC/chip?
(ii) Explain the techniques to reduce dynamic power near hot spots?
(iii) Explain the Threshold levels test in brief? **(3 M)**

Q2: Diagram shows IC with the dual ESD protection. Explain the mechanism to test pin to pin short. **(2 M)**



Q3: (i) List the types of golden vector test bench and also list its drawbacks compared to other test benches? **(2M)**

(ii) Explain the following control parameter in the On-the-Fly Random Test Cases. **(1M)**

DELAYCount:	**0**	**30**
	1	**25**
	2	**20**
	3	**15**
	4	**5**
	5	**5**

(iii) Explain separation of power on reset (POR) and mainline verification? **(1M)**

(iv) Discuss reusability with independent stimulus components for reusability by drawing environment diagram? **(1M)**

Q4: A calculator design has 4 input ports where each port may receive up to 4 outstanding commands of types NOP, ADD, SUB, SHL, SHR. The internal resources are one add/sub unit and one shift unit. The input consist of the request command <0:3>, request input data <0:31> (Operand1 data arrives with command, Operand2 data arrives on the following cycle) and request input tag <0:1>. The output has response line <0:1> (i.e. 00- no response, 01- successful operation completion, 10- invalid command or overflow/underflow error, 11 - Internal error), output data <0:31> having valid result data on output lines accompanies response in same cycle along with output tag <0:1>. The minimum number of cycles it takes to complete an operation are 3.
Draw the execution of operations, if all four ports are send with four SUB commands followed by a shift left command on port 1 for successful operation completion **(2 M)**

Q5:

(i) Perform the system behavioral verilog HDL code for 1 bit full adder using 'logic' data type. **(2M)**

(ii) Print the output of following system verilog program?

```
module PQR;
int abc[], xyz[];
initial
begin
abc=new[5];
foreach (abc[j])
 abc [j]= 10*j;
xyz=abc;
foreach (xyz[j])
 xyz [j]= abc [j]*2;
$display (abc[0], abc [1], abc[2], abc[3],abc[4]);
$display (xyz[0], xyz [1], xyz[2], xyz[3],xyz[4]);
 abc=new[10] (abc);
$display (abc[0], abc[2], abc[8],abc[9]);
abc.delete ();
end
endmodule
```

(3 M)

(iii) Write the output of following system verilog program after executing each line ? Also write the command to display these outputs? **(3 M)**

```
initial
begin
int y, x[ ] = '{2,19,4,11,8,13,4,2,8}, pq[$] ;
y=x.sum with ((item>7)*item*10);
pq=x.unique();
end
```

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