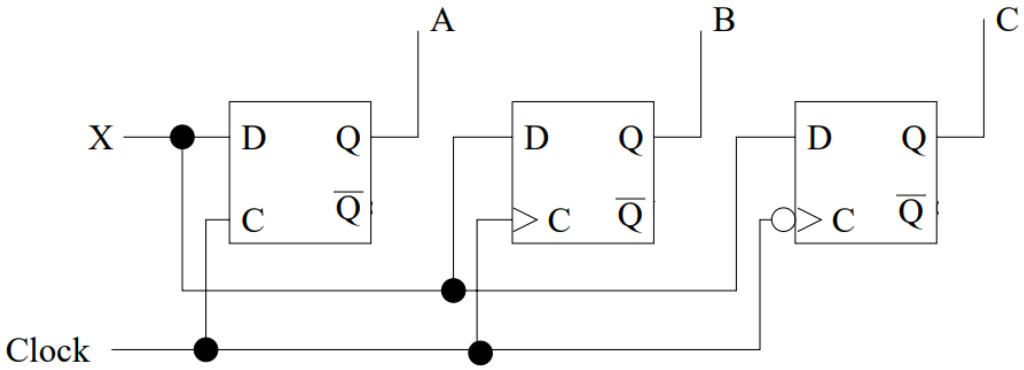
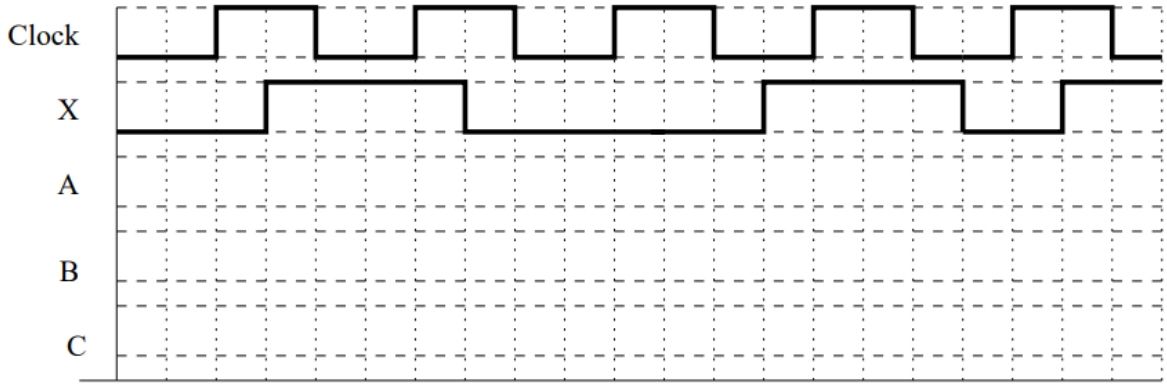
Birla Institute of Technology and Science, Pilani.
Comprehensive Examination: CS/EEE/INSTR F215: Digital Design
Marks: 40 AY: 2017-18, Semester: I Date: 05-December-2017, Tuesday
Time: 60 minutes CLOSED BOOK (Part-A) Pages: 02

BITS ID:_____ NAME:_____ SECTION:_____

Q1 The circuit below has three D flip-flops. Complete the timing diagram by filling in the waveforms for A, B, and C. **[8]**





Q2 Design and realize a mealy machine using minimum numbers of T flip-flops and logic gates to detect a sequence of 101 in a given input stream. The output goes high on correct detection of last bit of the given sequence. Consider overlapping condition. **[8]**

Q3 Draw the logic implementation of $\boldsymbol{y = f(a, b, c, d)}$ for the following Verilog description. Label all the inputs, output and wires. **[8]**

```
module gate (y, a, b, c, d)
input a, b, c, d;
output y;
wire w1, w2, w3, w4, w5, w6;
nand n1(w2, a, b, w3);
xor x1 (w1, c, d);
nor n2(w3, a, b, c, w1);
assign w5=w1^w2;
or o1(w6, w1, w2, w4);
and A1(w4, w5, d, a);
assign y=w5 & w6;
end module
```

Q4 Find the simplest SOP form of the function, $\boldsymbol{F = X.Y}$, where **[8]**

$$\boldsymbol{X = AB\overline{C} + \overline{C}D + \overline{A}C\overline{D} + \overline{B}C\overline{D}}$$

$$\boldsymbol{Y = (A + B + \overline{C} + \overline{D})(\overline{B} + \overline{C} + D)(\overline{A} + C + \overline{D})}$$

Q5 Implement the following function using **only** two 4:1 MUXs (logic gates not allowed). Use A, B and C as selector lines. $f(A,B,C) = A \oplus B \oplus C$. **[8]**

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Marks: 80 AY: 2017-18, Semester: I Date: 05-December-2017, Tuesday
Time: 120 minutes OPEN BOOK (Part-B) Pages: 01

Q1 (a) Draw transistor level implementation of Boolean function Y using CMOS logic family. **[20]**
Use minimum number of transistors and assume complementary inputs are available.

$$Y = \bar{A}D + \bar{B}(A + \bar{C})$$

(b) Realize the Boolean function Z using Transmission Gate logic (TG). Assume CMOS inverters and complementary inputs are available.

$$Z = \bar{A} + B\bar{C} + \bar{B}C$$

(c) Analyze and determine the Boolean expression implemented at output V_0 using TTL logic as shown in figure 1(a).

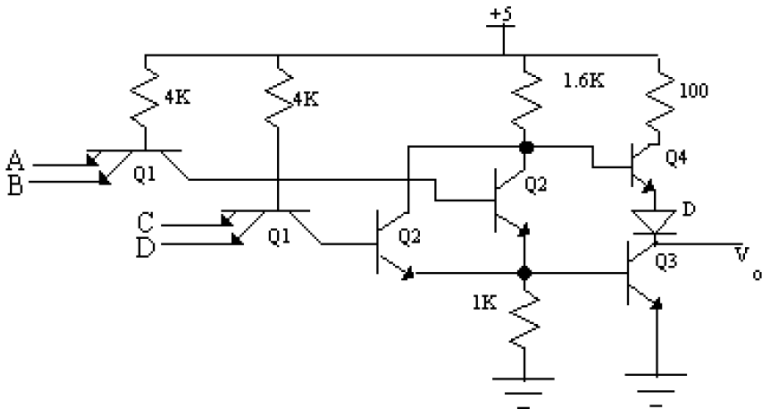

Fig 1(a): TTL Logic Circuit

Q2 A digital system is to be designed with the following specifications: At power on the circuit is in some initial state T_0 and on next clock edge clears a 4-bit Register (**R**), 4-bit counter (**C**) and a flip-flip (**E**) and goes to next state T_1. In T_1 register **R** is loaded with user defined 4-bit data and circuit moves to next state T_2. In T_2 counter (**C**) starts counting up. When the **C** value is equal to **R** value, **E** is set on next clock pulse and circuit returns to T_0. **[20]**

a. Design a ASM chart for the above problem
b. Design Controller using one-hot state assignment
c. Design the datapath required with all status and control signals

Q3 Design a circuit which has as 4-bit input W [3:0] and 9-bit output X [9:0] where both are treated as 2's complement numbers. Design a logic circuit to make X equal to 6 times W's value. You may **only** use: • One 8-bit **adder** (with carry in and carry out) • Three **NOT** gates • Power and ground. **[20]**

Q4 Design a circuit shown in fig 4(a) which generates waveform at output Z. The output Z changes with every clock cycle in the following pattern shown in fig 4(b): **[20]**

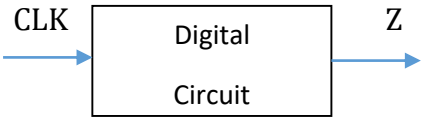

Fig 4(a): Digital Circuit

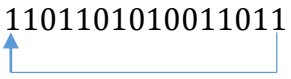

Fig 4(b): Pattern

Design the circuit using **only** following components:
• One **4:1 MUX** with active high enable. • One **2:4 Decoder** with active high outputs and active high enable. • Any number of 2-input and 4-input **OR** gates. • Two 2-bit binary **UP counter** with asynchronous clear. Two 2-input **AND** gates.