Birla Institute of Technology and Science, Pilani.
Mid-Semester Examination: CS/EEE/INSTR F215: Digital Design
Marks: 90 AY: 2017-18, Semester: I Date: 10-October-2017, Tuesday
Time: 90 minutes CLOSED BOOK Pages: 01

Note: Attempt all parts of a question together

Q1 For the given Boolean expression $F(A,B,C,D) = \sum m(0,1,3,6,8,10,12,14) + \sum d(5,9,13,15)$. Where ***A*** is MSB and ***D*** is LSB **[20]**

a) Plot the K-map.

b) Identify the Prime Implicants (PI). Express each PI as product form.

c) Identify Essential Prime Implicants (EPI). Express each EPI as product form.

d) Write down expression for all the possible minimal SOP's of output function **F**.

e) Draw the two level circuit diagram of the minimal SOP (any one) using NAND gates. Assume inputs are available in true and compliment forms.

Q2 Realize F_1 and F_2 using a minimum size PLA. Give the size of and draw PLA table. **[10]**

$$F_1(W,X,Y,Z) = \sum m(1,2,4,5,6,8,10,12,14)$$

$$F_2(W,X,Y,Z) = \sum m(2,4,6,8,10,11,12,14,15)$$

Q3 a) Realize the following function ***F*** using only ONE 4:1 multiplexer with active high enable. Only true (uncomplimeted) inputs are available. **[20]**

$$F(W,X,Y,Z) = \sum m(3,4,5,7,10,14) + \sum d(1,6,15)$$

Q4 Design and realize a 2-bit magnitude comparator circuit as shown in figure 1, using **only** minimum numbers of Multiplexers (4:1) and Decoders (2:4). Assume enable of both components are active high and outputs of decoders are active high. **[20]**

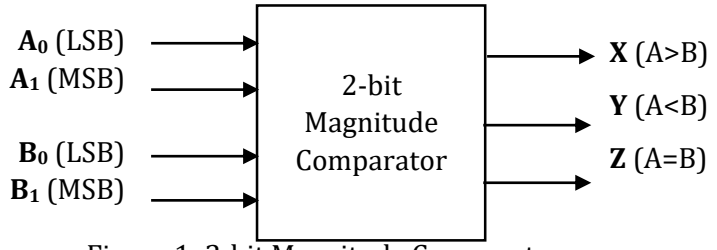

Figure 1: 2-bit Magnitude Comparator

Q5 Design a single Mealy machine to detect the sequence 1001 and 010 in a given input stream. The circuit has one serial input X and one output Z. The output goes HIGH on correct detection of last bit of any of the given sequences. Consider the overlapping condition. Realize the Mealy machine using minimum number of D flip-flops and external logic gates. Draw a Mealy state diagram and Mealy state table. Assume unused states (if any) as don't care. **[20]**