ID Number:_____ Name: _____

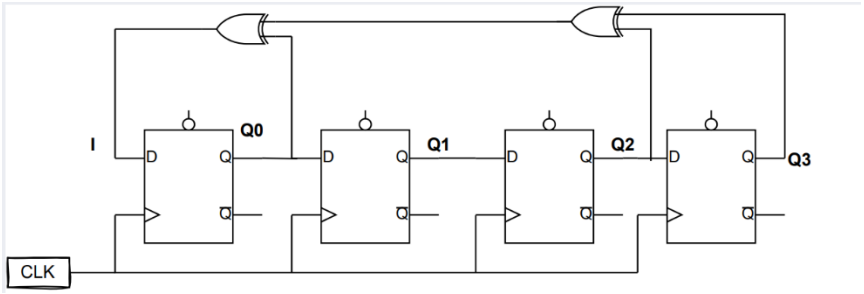
Birla Institute of Technology and Science, Pilani.
Comprehensive Examination: CS/ECE/EEE/INSTR F215: Digital Design
Marks: 40 AY: 2022-23, Semester: I Date: 21-December-2021, Wednesday
Time: 60 minutes CLOSED BOOK Pages: 02

Q1	Implement the function $F(A,B,C,D,E) = \Sigma m(1,2,5,6,8,11,12,15,17,18,21,22,24,27,28,31)$ using ONE 4:1 MUX and ONE XOR gate. Only true form of inputs is available.	**[5]**
Q2	Draw the PAL Programming table for a PAL of suitable size to generate the 3 function outputs F1, F2, and F3 where F1(A,B,C)=Σm(0,1,3,5,7) F2(A,B,C)= Σm(2,3,6,7) and F3(A,B,C)= Σm(0,4,5,6).	**[5]**
Q3	Implement the function $F(A,B,C,D) = \Sigma m(0,5,10,15)$ using only **ONE** 1:4 **DMUX**, and required numbers of half adders only. Inputs are available in true form only.	**[5]**
Q4	Implement the function $F(A,B,C,D) = \Sigma m(3,4,5,6,9,10,11,12)$ using minimum numbers of transmission gates. Inputs are available in TRUE and COMPLIMENT form.	**[5]**

Q5 Implement the following function using minimum number of CMOS transistors. Inputs are available in true form only. $F = \overline{A}\,\overline{B}\,\overline{D} + \overline{C}\,\overline{D}$ **[5]**

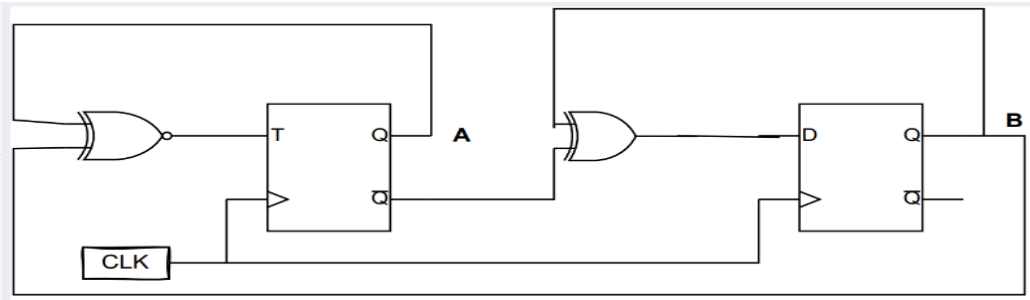
Q6 Design a clocked sequential synchronous counter which counts 0→1→3→7→6→4→0, using only positive edge triggered D-Flip-Flops. **[5]**

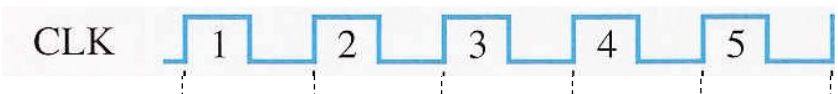
Q7 A 4-bit right shift register is initialized to a value 1000 for Q3, Q2, Q1, Q0. The input I is derived from Q0, Q2 and Q3 as shown in the figure. What will be the value of Q3, Q2, Q1 and Q0 (IN BINARY FORMAT) for 5 clock pulses after initialization. **[5]**



CLK	Q3	Q2	Q1	Q0
INT	1	0	0	0
I				
II				
III				
IV				
V				

Q8 A circuit with T-FF and D-FF is shown on the right. Draw the waveforms for A and B for 5 clock pulses. Initially A=B=0 **[5]**





A

B

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Q1	An AB flip-flop operates as follows: If $\boldsymbol{A = B = 0}$, the flip-flop state $\boldsymbol{Q = 0}$; if $\boldsymbol{A = 0}$ ***and*** $\boldsymbol{B = 1}$ the flip-flop state $\boldsymbol{Q =}$ ***No change***; if $\boldsymbol{A = 1}$ ***and*** $\boldsymbol{B = 0}$ the flip-flop state $\boldsymbol{Q =}$ ***Toggle***; and when both $\boldsymbol{A = B = 1}$, the flip-flop state $\boldsymbol{Q = 1}$. (a) Construct the state table and derive the characteristic equation for this AB flip-flop. (b) Convert JK flip flop to AB flip-flop. Realize the circuit using the JK flip-flop and 2-input NAND gates only. (c) Use the obtained AB flip-flop to design a 4-bit binary asynchronous mod-6 down counter. Assume the initial state of the counter (WXYZ; W: MSB and Z: LSB) as 1111. The AB flip-flop has synchronous and active low PRESET and CLEAR pin. Apart from AB flip-flop, 2-input NAND gates are available for design. Use only required number of NAND gates. Inputs are available in only TRUE form. (d) Using required number of AB flip-flop(s), design a non-sequential counter which counts as 0-6-5-3-2-1-0 and repeat. Apart from AB flip-flop, 2-input NOR gates are available for design. Use only required number of NOR gates. Inputs are available in only TRUE form. Assume counter outputs as $Q_n \dots \dots Q_2, Q_1, Q_0$. Where Q_n: MSB and Q_0: LSB	[20]
Q2	A logic circuit realizes a function $F(A, B, C, D)$. The three inputs $\boldsymbol{A}, \boldsymbol{B}$, and $\boldsymbol{C}$ are the binary representation of the digits 0 through 7 with $\boldsymbol{A}$ being the **MSB**. The input $\boldsymbol{D}$ is an odd-parity bit; that is, the value of $\boldsymbol{D}$ is such that $\boldsymbol{A}, \boldsymbol{B}, \boldsymbol{C}$, and $\boldsymbol{D}$ always contains an odd number of 1's. The function $\boldsymbol{F}$ has value 1 if the input digit is a prime number. (A number is prime if it is divisible only by itself and 1; 1 is considered to be prime, and 0 is not). Consider output as don't care for invalid inputs. (a) Draw a Karnaugh map for F. (b) Find all prime implicants and Essential prime implicants of F. (c) Find all minimum sum of products for F. Realize the minimum SOP using only required numbers of 2-input NAND gates. (d) Find all prime implicants and essiential prime implicants of $\bar{F}$. (e) Find all minimum product of sums for F. Realize the minimum POS using required numbers of 2-input NOR gates only.	[20]

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Q3	A battery charging indicator system needs to be designed using Moore sequential circuit. Input to the system is charging current measured through a 4-bit analog to digital converter, whose output is available in a 4-bit register M. Register M can be loaded into another 4-bit register A for internal use of the system. Input also consists of a switch S (if S=0, charging circuit is off, else it is ON). Output of the system consists of 3-bit register B (B= B2B1B0) connected to a RGY LED. If B = 000, then LED is OFF, if B = 001 then LED glows green, if B = 010 then LED glows yellow, and if B = 100 then LED glows red. LED glows based on value of charging current. If value of charging current is greater than Imax then LED blinks red (indicating fault), else if charging current is less than Imin then LED glows green steadily (indicating full charge), else the LED glows yellow steadily (indicating normal charging). A clock pulse at twice of the frequency of blinking is available for the design. If S=0, then system should be reset immediately, with LED in OFF condition and detection of fault should be on priority. Assume that value of Imax and Imin is preloaded in registers as I_MAX and I_MIN respectively. Measured current value should be appropriately loaded in register A and A can be compared with Imax and Imin using two 4-bit comparators within same clock. The desired outputs of comparators are denoted as X and Y (If A>Imax, X=1, and if A<Imin, Y=1). (A) Draw the ASM chart for the above design with proper labels and neatness. (B) Write state equations for the design using one-hot coding.	[20]
Q4	Design an octal to binary priority encoder and realize it using minimum number **4:1 MUX** only. The designed priority encoder must have active high outputs. Inputs are available only in True from. Assume encoder inputs as (D7, D6, D5, D4, D3, D2, D1, D0) D7 as MSB and D0 as LSB Encoder outputs as (B2, B1, B0) B2 as MSB and B0 as LSB	[20]