

**Computer Architecture (CS F342)**  
**Semester-I, 2022-23**  
**Comprehensive Examination**  
**Department of Computer Science and Information Systems (CSIS)**  
**BITS-Pilani, K K Birla Goa Campus, Goa, India.**  
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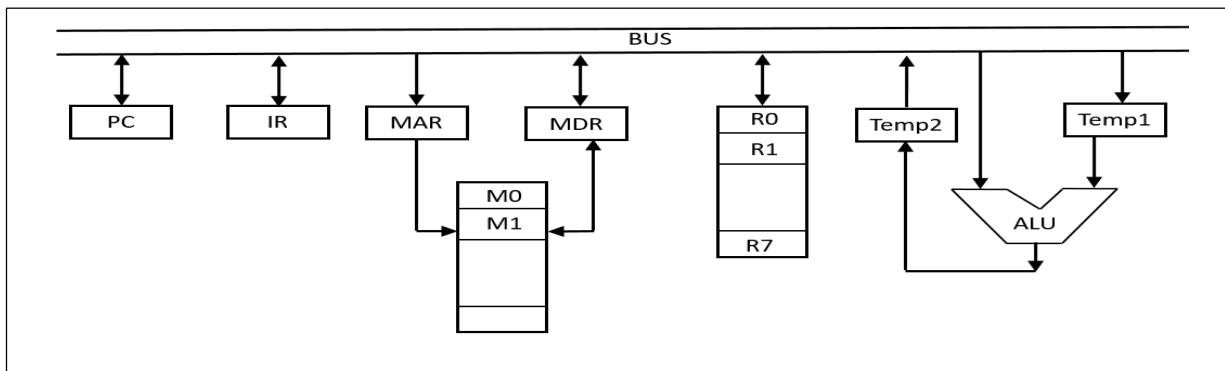
**Date: Dec 28, 2022: 10:00 AM**

**Duration: 3 Hrs**

**Instructions:**

**For the questions, no marks would be awarded if no reasoning is found in the answer script. You must write all answers of a question contiguously [not here and there within the answer script].**

1. (a) Why does the MIPS microprocessor perform the left-shift-by-2 operation in the BNE instruction and not in LW or SW instruction?
- (b) How does 5 stage pipelined MIPS microprocessor resolve the dependency in H/W level between 5th stage and 2nd stage? Describe the concept only with some specific terminology used in MIPS.
- (c) Which stages have the dependencies if branch decision is taken at 2nd stage instead of 3rd stage of 5 stages MIPS microprocessor, and how does one resolve such dependencies? Describe the concept only with some specific terminology used in MIPS.
- (d) Can we program the stage registers and registers in the 2-level branch predictor in 5-stage MIPS microprocessor directly? Justify your answer.
- (e) Consider the following datapath diagram and an instruction, ADD R0, R1, R2 ( $R0 \leftarrow R1 + R2$ ).



The following steps are used to execute the instruction mentioned above over the given data path. Assume that PC is incremented appropriately. The subscripts  $r$  and  $w$  indicate read and write operations, respectively.

1.  $R2_r$ ,  $TEMP1_r$ ,  $ALU_{add}$ ,  $TEMP2_w$
2.  $TEMP2_r$ ,  $R0_w$
3.  $MDR_r$ ,  $IR_w$
4.  $R1_r$ ,  $TEMP1_w$
5.  $PC_r$ ,  $MAR_w$ ,  $MEM_r$

Write down the execution of the steps.

**Marks: Each part (a), (b), (d) and (e) carry 17%, and part (c) carries 32% of marks**

2. (a) Do process context switches, a concept in Operating Systems, affect the branch prediction's accuracy? Does mapping order in the page table affect the branch prediction? Justify your answer.
- (b) Consider the following C-program snippet. The variable  $i$  and  $j$  are integer types. How many cycles are required to run the following program on the simple 5 stage pipelined 32-bit MIPS processor? What is the CPI of this program? Show the detailed steps to solve the problems and your assumption.

```

for (i=0; i<6; i += 3){
    for (j=5; j>0; j - = 1){
        ;
    }
}

```

(c) Derive the general equation for determining the trade-off between cost and performance for designing the pipelined-based microprocessor. Describe all steps clearly.

**Marks: Each part (a) and (c) carry 30%, and part (b) carries 40% of the marks**

3. Manually design [draw the datapath and controller table] the 32-bit single-purpose processor which executes the following algorithm:

```
W=0, X=0, Y=0
INPUT Z
WHILE (Z != 0){
    W = W - 2
    IF ( Z is an odd number ) THEN
        X = X + 2
    ELSE
        Y = Y + 1
        Z = Z - 1
}
```

Use only one adder-subtractor unit for all of the addition and subtraction operations. Highlight & count the control and status signals in the datapath for such a processor.

4. Write an ASM program using MIPS ISA for the above-mentioned algorithm and find the dependencies [data & control] with the instruction of window size one.

**Marks for 3 & 4: 70% and 30% of the marks.**

5. We want to add the swap instruction, *swap rs, rt*, in the Single-Cycle MIPS microprocessor. The interpretation of the instructions is  $\text{Reg}[rs] = \text{Reg}[rt]; \text{Reg}[rt] = \text{Reg}[rs]$ .

- (a) Show the [optimal] modification in the microprocessor's datapath. More precisely, only the modified part, **not the entire datapath**. Show the modification in the controller, i.e., only the table for the new instructions.  
(b) Compute the *swap rs, rt* using other instructions of MIPS ISA.

**Marks: The two parts carry 70% and 30% of the marks.**

6. (a) Consider the program's reference pattern of accessing the blocks 0, 4, 0, 8, 0, 8, 0, 4, 0, 4, 0, 4. Assuming that the set size is 2, find the hit ratio with a cache size of four cache lines and LRU replacement policy. Show all the steps in the calculation of the hit ratio.  
(b) Why is it called a pseudo-LRU algorithm? Explain it as a case for 3-bit PLRU.

**Marks: The two parts carry 30% and 70% of the marks.**

**-: End :-**