BIRLA INSTITUTE OF TECHNOLOGY & SCIENCE, PILANI
I SEMESTER 2023-2024
CS F342 COMPUTER ARCHITECTURE
COMPREHENSIVE EXAM PART B (CLOSE BOOK)

TIME: 90 Min. **07/12/2023** **MM: 45**

Q1. (a) A RISC Processor having a five stage pipeline as discussed in class is used. The Pipeline hardware detects all possible data hazards and stalls the pipeline when necessary for correct program behavior (no forwarding). For such a Processor draw cycle by cycle execution schedule (Pipeline diagram) in the pipeline for the following program for one iteration of the loop through this pipeline. Find the CPI and MIPS rating if the machine is running on a 4GHz clock. **[12]**

```
LOOP:   LW      R1,     4(R2)
        ADD     R2,     R2, R3
        SUB     R3,     R2, R1
        SW      R3,     6(R3)
        SW      R4      6(R4)
        OR      R1,     R4,R3
        BEQ     R3,     R4, LOOP
```

(b) Unroll the loop once. Reschedule the code to minimize the stalls. Assume only one extra register (R8) is available. Find the new CPI and MIPS rating. (Assume that number of iterations of the original loop are multiple of 2).

Q2. (a) Using Tomasulo's algorithm, for each instruction in the following sequence determine when (in which cycle, counting from the start=1) it **issues, begins execution, ends execution and writes its result to the CDB**. ***Assume that the result of an instruction can be written in one cycle after end of its execution***. The execution time of all instructions is three cycles, except for multiplication (which takes 4 cycles) and division (which takes 6 cycles). The processor has multiply/divide units and add/subtract units. The multiply/divide unit has two reservation stations and the add/subtract unit has three reservation stations. There are one load and one store reservation stations as well. Assume that at start all instructions are already in the instruction queue, but none has yet been issued to any reservation stations. The processor can issue only one instruction per cycle, and there is only one CDB for writing results. In case of tie the instruction which is issued earlier will get the CDB first.
(b) For the execution is part (a) show the contents of 'Register Result Status' at all instances where its contents are changed. **[12]**

```
LD.D F2, 0(R1)
MUL F4,F2,F0
MUL F6, F8, F10
DIV F12, F4, F6
ADD F14, F16, F18
SUB F20, F14,F6
SD.D F14, 4(R1)
SUB F20, F14,F22
```

Q3. Consider a computer with a 12-bit address space and a two level cache. The parameters of the caches are as follows:

- L1: 32 bytes, direct mapped, 8-byte cache lines.
- L2: 512 bytes, 4-way set associative, 32-byte cache lines. LRU replacement policy

(a) Show the address division for the two levels

(b) The table below shows a trace of memory accesses (loads) made by the processor. For each access specify whether it is a level 1 cache hit (Ll), a level 2 cache hit (L2), or a miss (M). Assume that initially all cache lines are invalid. [Draw a similar table in your answer sheet]. Show your work. **[11]**

Load No.	Binary Address	L1, L2 or M
1	1011 0101 0111	
2	1100 0111 0101	
3	1110 1111 1100	
4	1011 0101 0000	
5	1011 0101 1100	
6	1011 0101 0010	
7	1011 0111 1010	
8	0001 0111 1001	
9	1100 0101 0000	
10	1111 0111 1111	
11	1100 0111 0111	

Q4. The microprogram for the multicycle implementation of control unit as discussed in class is shown below.

Label	ALU control	SRC1	SRC2	Register control	Memory	PCWrite control	Sequencing
Fetch	Add	PC	4		Read PC	ALU	Seq
	Add	PC	Extshft	Read			Dispatch 1
Mem1	Add	A	Extend				Dispatch 2
LW2					Read ALU		Seq
				Write MDR			Fetch
SW2					Write ALU		Fetch
Rformat1	Func code	A	B				Seq
				Write ALU			Fetch
BEQ1	Subt	A	B			ALUOut-cond	Fetch
JUMP1						Jump address	Fetch

Dispatch ROM 1		
Op	Opcode name	Value
000000	R-format	Rformat1
000010	jmp	JUMP1
000100	beq	BEQ1
100011	lw	Mem1
101011	sw	Mem1

Dispatch ROM 2		
Op	Opcode name	Value
100011	lw	LW2
101011	sw	SW2

Write the microcode to implement the MCOPY (opcode=101010) function. The R-type format is used for coding the instruction. The instruction does the following:

MCOPY (rd),(rs),(rt) # Memory[R[rd]+ R[rt]] ← Memory[R[rs]+ R[rt]];

Where in the microprogram should the microcode for MCOPY be inserted? Draw all the relevant tables with the changes identified. (You have to draw only the changes in terms of additional rows/new tables inserted) **[10]**