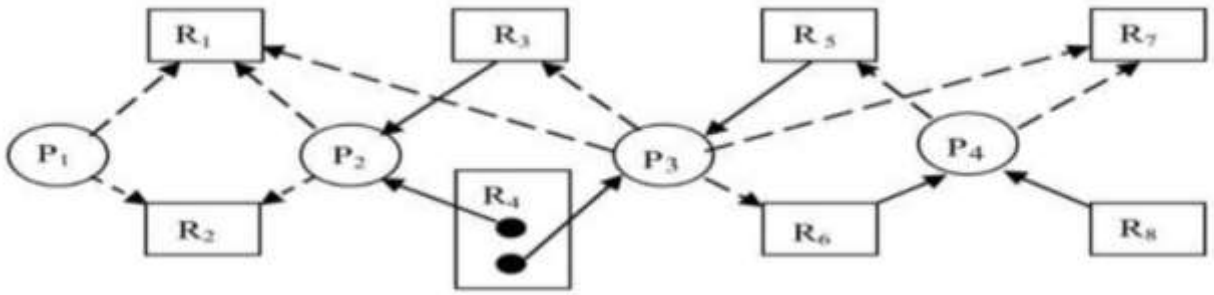
Birla Institute of Technology & Science, Pilani, Pilani Campus
II Semester 2022-2023
CSG523 Software for Embedded Systems
Mid-Semester Examination (Closed Book)

Date:14-3-2023 **Duration: 90 Minutes** **Max Marks: 25**

Q.1. What is stack underflow and mention at least one cause of stack underflow in an embedded system. Mention a method of detecting stack overflow as early as possible in an embedded system? Which of the peripherals of a microcontroller will you use for the same? **[3]**

Q.2. Based on the resource allocation graph for an embedded system shown below, is there a deadlock at the current instant? Is there a possibility of deadlock in future? How will you avoid deadlock through resource planning or resource allocation for the scenario given below. **[2]**



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Q.3. For an ARM Cortex M4 based microcontroller if the premption priority is represented by 3 bits and sub-priority is represented by 1 bit. **[2]**
Suppose there are 4 exceptions to be configured. E1, E2,E3,E4 for an application.
E1 and E2 should be assigned the same priority level but if both are raised simultaneously E1 should be served first by the processor.
E3 and E4 should be assigned the same priority level but if both are raised simultaneously E3 should be served first by the processor.
E1 or E2 should be served first by the processor when compared to E3 and E4.
Mention the values that should be configured into the NVIC interrupt priority registers for configuration of priorities for each exception (E1, E2, E3, E4) as per the requirement.

Q.4. Write an Assembly program for ARM Cortex M4 based application to set all even bits of a variable "dat1" mapped to a SRAM location 0x20000000 while keeping the rest of the bits of variable unchanged using BIT banding. The bit band region starts from 0x20000000 and the bit band alias region starts from 0x22000000. **[3]**

Q.5. ARMv7 architecture implements several features which reduces interrupt latency. For an application based on ARMv7 architecture four interrupts IRQ0, IRQ1, IRQ2 and IRQ3 are initialized in the system. Hardware Priority order is IRQ0>IRQ1>IRQ2>IRQ3.
Assume that initially interrupt IRQ 2 and IRQ1 are generated simultaneously in a system. The processor is in Thread unprivileged mode using PSP when the interrupts are raised initially.

While IRQ1 is being serviced, interrupts IRQ0 and IRQ3 are generated simultaneously. Indicate the number of stacking and unstacking which will occur during the execution of all 4 interrupts mentioned above using a stacking/unstacking diagram. Also indicate the stacks used for each stacking and un-stacking. **[3]**

Q.6. **[2+2]**

(a) You are required to define/declare a memory mapped register (address : 0x48000000) by casting the address to a pointer and initialize the register with a value of 10 (decimal). Write the code snippet for above mentioned definition and for initialization of the location.

(b) const volatile int * const val= <initial value>;
What is the use/significance of the qualifiers const (first and second const) and volatile in the object description. Is the declaration given above a valid description?

Q.7. Write a pseudocode for heap memory allocation and deallocation for a system with fixed-sized memory pools for heap management in an embedded system.
Is the possibility of external fragmentation reduced or increased while using fixed-sized memory pools for heap management when compared to having the same-sized memory blocks in the heap? Justify your answer. **[3+2]**

Q.8. A static variable is not necessarily a global variable. Do you agree with the statement? Justify your answer with an example. **[1]**

Q.9. Suppose a task A is running in Thread Unprivilged mode in for an ARM Cortex M4 based processor. Mention the steps required to resume the execution of task A in Thread privileged mode. **[2]**

Additional Information:

Execution return codes:

0xFFFFFFF1 – Return to handler Mode

0xFFFFFFF9 – Return to thread mode using MSP

0XFFFFFFFD – Return to thread mode using PSP