Advanced Computer Architecture (CS G524)
Semester II, 2022-23
Mid-semester Examination
Department of Computer Science and Information Systems (CSIS)
BITS-Pilani, K K Birla Goa Campus, Goa, India.

Mar 18, 2023: 11 am Duration: 1 hr 30 mins # of Questions: 3 Marks: 40 [7 + 25 + 8]

Instructions: **Attempt all the questions. No marks will be awarded for the questions if no reasoning is found in the answer script. You must continuously write all answers to a question [not here and there within the answer script].**

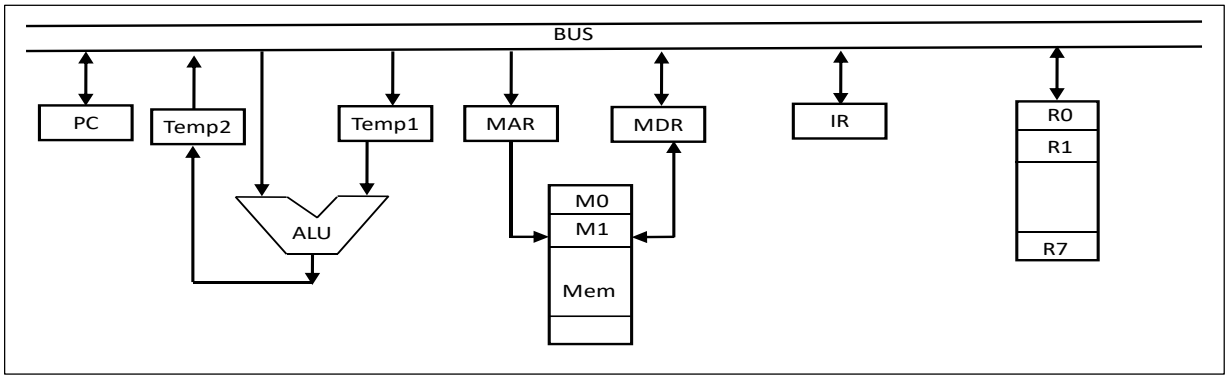
1. (a) What is the role of the architectural and non-architectural elements in the datapath of a processor?

(b) What's the role of the ALUOut register in the Multi-cycle non-shared-bus MIPS microprocessor for the BEQ or BNE instruction?

(c) Are we storing the PC + 4 in ALUOut register for updating the PC in the Multi-cycle non-shared-bus MIPS microprocessor? Justify your answer.

(d) Find out the width of the control memory of a horizontal microprogramming control unit for the following configuration: Conditional branching needs 8-bit status, 10 control lines for the processor of ALU and 32 registers, and provision to hold 128 words in the control memory.

(e) Consider the following datapath diagram and an instruction, SUB R0, R1, R2 (R0 ← R1 - R2).



The following steps are used to execute the instruction mentioned above over the given data path. Assume that PC is incremented appropriately. The subscripts *r* and *w* indicate read and write operations, respectively.

1. PC_r, MAR_w, MEM_r 2. MDR_r, IR_w 3. $R1_r$, $TEMP1_w$ 4. $TEMP2_r$, $R0_w$ 5. $R2_r$, $TEMP1_r$, ALU_{sub}, $TEMP2_w$

Write down the order of the execution of the steps.

[**Marks**: 1 + 1.5 + 1.5 + 2 + 1]

2. Design a system for the continuous incoming bits (0/1). The system will provide output "1" if it processes an even number of 1s. Otherwise, the system will produce output 0. It will produce output "1" at the start of the system. Describe the system using:
(a) Verilog HDL [input is coming from testbench, write the code for main and testbench module],
(b) C [input is coming from a file, and spaces separate them],
(c) MIPS ASM [input is coming from a keyboard] by assuming that a basic 5-stage pipeline MIPS microprocessor also counts the number of instructions and execution cycle of your program.
(d) Find out the execution cycle of the program you wrote for part (c) for the Single and Multi-cycle MIPS microprocessor.
(e) Design the hardwired control unit [block diagram with dimension & logical expressions] to generate control signals for the system.

[Marks: 7 + 3 + 9 + 2 + 4]

3. Designer wants to add a new instruction, *branch-on-bit-set (BBS)*, in the existing 32-bit Single-Cycle MIPS ISA. The instruction, *BBS src, pos, label*, jumps to the *label* if the bit position in the *pos* of the *src* register is "1". Help the designer modify the datapath and control unit [answer only the modified parts] and show the ALU operation using Verilog HDL. Make your assumption properly.

[**Marks**: 8]