Note: Answer all the questions in the same sequence.

1. Explain in brief (not more than a single sentence), how each of the following drawbacks of Von Neumann computing paradigm are addressed in modern day computing systems. **[6M]**
    (i)   Speed efficiency issue: Von Neumann uses sequential program execution.
    (ii) Resource efficiency issue: only a part of the hardware resources is required for execution of an instruction. Rest of the resources remain idle.
    (iii) Memory access issue: The memory devices (specifically those used as Main memory) are slower than the processor.

2. Classify each of the following reconfigurable computers as fine grained or coarse grained architecture and justify your answers (in a single sentence).
    (i) RaPiD   (ii) GARP   (iii) Chimera **[3M]**

3. Draw the reduced Binary Decision Diagram (BDD) for the function $F = (A + \bar{C}).(B + C)$ (use order A,B,C). (Draw the complete BDD from truth table and optimize it) **[6M]**

4. A unidirectional switch matrix is shown in the figure below. Ain, Bin, Cin and Din represent the inputs (represented as ● in the figure) and Aout, Bout, Cout and Dout represent the outputs (represented as ○ in the figure) of the switch matrix. As seen from the figure, each output can be connected to three possible inputs. Show the detailed circuit implementation for Cout generation (only) using **pass transistor** based programmable interconnects. Also, determine the total number of bits required to program the complete switch matrix. **[5M]**

5. For the CMOS circuit shown in figure below, determine if each of the transistors (M1, M2, M3…M9) is ON or OFF and also the find logic value of "**Out**", for all possible logic values of **A, B**. **[8M]**

(your answer should be in tabular form as shown below)

A	B	M1	M2	M3	M4	M5	M6	M7	M8	M9	Out
0	0	ON/OFF	ON/OFF	ON/OFF	ON/OFF	ON/OFF	ON/OFF	ON/OFF	ON/OFF	ON/OFF	0/1
..	..										

6. While designing a new PE (programmable element) structure, designers have to make a choice between using a small size LUT with additional elements or a large size LUT. Assume that your manager has asked you to design a combinational 3-input, 3-output PE structure, which is optimal for implementation of a 4-bit incrementer circuit (Assume $A(A_3A_2A_1A_0)$ as input and $O(O_3O_2O_1O_0)$ as output. If input is 0000, incrementer output will be 0001)

Initially, you have come up with two different designs. Figure 6(a) shows first design with one 2-input, 3-output LUT and two 2:1 multiplexers. Figure 6 (b) shows second design with just one 3-input, 3-output LUT and no additional elements.

To determine which PE design is better, implement a 4-bit incrementer optimally using

(a) least number of PEs, when PE structure is as shown in Figure 6(a)

(b) least number of PEs, when PE structure is as shown in Figure 6(b)

Comment on advantages and disadvantages of both the PE designs with respect to the implementation of 4-bit incrementer. **[12M]**

(Full marks will be awarded only if the designs are optimal and use least number of PEs. Partial marks may be given for correct implementations which are not optimal and/or use more PEs. For each circuit implementation, show the interconnection between PEs clearly and for each LUT, instead of truth table, mention the logic function implemented by outputs as a function of inputs)
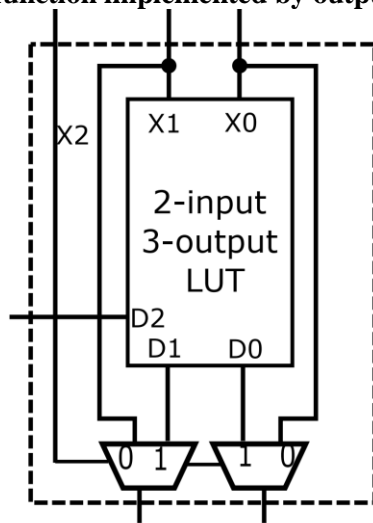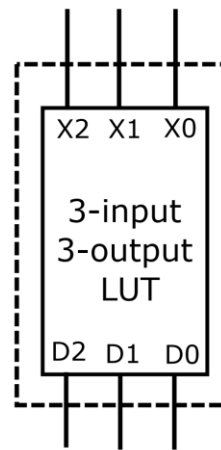

Figure 6(a): PE Design 1

Figure 6(b): PE Design 2