

Note: Answer all the questions in the same sequence.

1. (i) List the three different control flow based transformations that are used for optimization in the high level synthesis. Given example for each transformation. [3M]

(ii) Answer the following questions with respect to GARP Reconfigurable processor

- (a) List the four different major category (type) of operations that can be implemented in the logical/arithmetic functional block of GARP processor. [4M]
- (b) Calculate the number of configuration bytes required for GARP processor which has 48 rows of PEs (processing elements) [2M]
- (c) How many VICs (Virtual Instruction Configurations) can be stored in the configuration cache of GARP processor. [2M]
- (d) List the different types of re-configuration supported by GARP processor. [2M]

2. Represent the following code using FSMMD representation [8M].

```

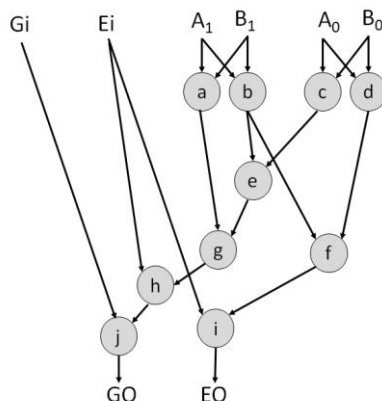
for (i=0; i<n; i++)
{
    if (i==0)
    {
        A[i]=0;
    }
    else
    {
        if (i==1)
        {
            A[i]=1;
        }
    }
    if (i>1)
    {
        A[i] = A[i-1] + A[i-2];
    }
}
    
```

3. Show the generic block level implementation (label all inputs, outputs) of any arbitrary 6-input function $F(x_0, x_1, x_2, x_3, x_4, x_5)$ (i.e. any 6-input function) using minimum number of elements under the following constraints:

- (i) Only 3-input LUTs are available
- (ii) 3-input LUTs and Seven 2:1 multiplexers are available
- (iii) Only 4-input LUTs are available

Determine the number of LUTs required for each of the above three cases. [17M]

4. For the Boolean network shown below ($G_i, E_i, A_1, B_1, A_0, B_0$ are Primary Inputs and G_0 and E_0 are Primary Outputs), apply the flow-map algorithm to find the LUT mapping (for $K=3$ i.e. 3-input LUT). Show all the steps. Show the node labeling analysis for each node and the final node mapping (LUT Mapping) for the nodes. Show the final LUT based circuit and in each LUT mention the nodes that the LUT maps. [18M]



5. Consider the Boolean expressions given below

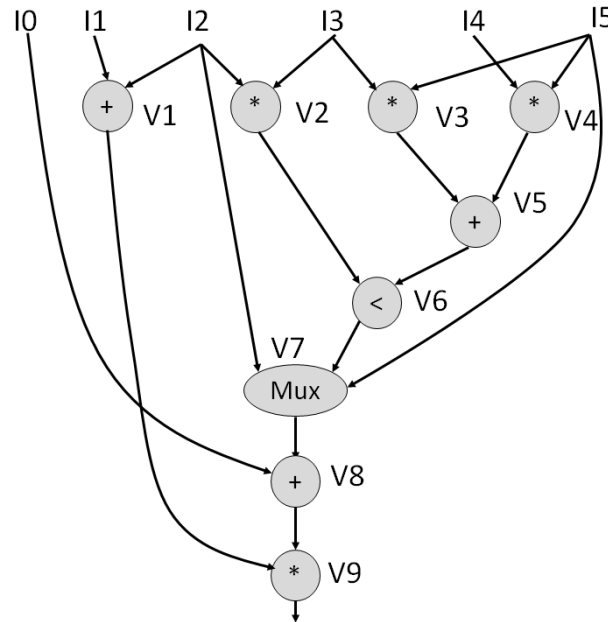
(a) $F1 = (A \odot B)AB + (A \oplus B)\bar{C}$

(b) $F2 = AB + BC + CA$

For each of the above equations,

- (i) Draw the Ordered BDD directly from equations (without using the truth table) with ordering as $A \rightarrow B \rightarrow C$. Reduce the OBDD in obtain ROBDD
- (ii) Based on ROBDD, check if the above Boolean expressions are equivalent. [8M]

6. Consider the data-flow graph shown below:



Assume the following parameter values for FPGA implementation:

- Multiplication requires 50 clock cycles, Addition requires 20 clock cycles, comparison requires 15 clock cycles and the multiplexing operation requires 10 clock cycles.
- Multiplier requires 100 LUTs, Adder requires 20 LUTs, comparator requires 10 LUTs and the Multiplexer requires 8 LUTs.

- (a) Draw the sequencing graph for the above data-flow graph. [2M]
- (b) For an FPGA with 150 LUTs, apply list scheduling based temporal partitioning algorithm for partitioning the sequencing graph in (a). (Assume priority is assigned based on number of successors) (Clearly show which nodes are mapped to which partition) [5M]
- (c) Calculate the quality of the partitioning obtained in (b). [2M]
- (d) Calculate the wasted resources for the partitioning obtained in (b), by clearly showing the graph of LUT utilization with respect to run time for each partition (For each node in a partition, mark LUT usage on X-axis and runtime on Y-axis). [7M]