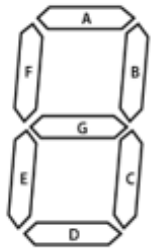
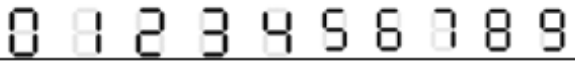
Birla Institute of Technology and Science, Pilani.
Mid Semester Examination: CS/ECE/EEE/INSTR F215: Digital Design
Marks: 90 AY: 2023-24, Semester: I Date: 13-October-2023, Friday
Time: 90 minutes CLOSED BOOK Pages:01

Information for Question 1 to Question 4:

A digital circuit takes a BCD number (WXYZ, W: MSB, Z: LSB) as input and displays its equivalent decimal number on a seven-segment display. The seven display segments are named (A - G) as shown in the figure. The segment is ON if the input is logic "1" and OFF if the input is logic "0". Assume that the unused inputs can be treated as don't cares. The BCD numbers (0-9) are displayed as below:





Q1 Plot the K-map for a single segment "C" of the seven-segment display for the BCD input. List all the Prime Implicants (PI's), Essential Prime Implicants (EPI), and minimum SOP forms. Realize the obtained expression using minimum numbers of 2-input NOR gates only. TRUE and COMPLEMENT inputs are available for design. [12]

Q2 Obtain the minimum size PLA for the two functions (F1 and F2) represented by segment "A" and segment "B" respectively. PLA outputs are available in TRUE and COMPLEMENT form. Draw PLA table only. [10]

Q3 Realize the function (F3) represented by segment "E". Choose the required components from the list. Only TRUE inputs are available for design. [10]

- **TWO** 2-to-4-line decoders with active high output and one active-high enable
- **ONE** 4-to-2-line encoder with active high output and active high enable

Q4 Realize the function (F4) represented by segment "F". Choose the required components from the list. Only TRUE inputs are available for design. [10]

- **ONE** 4:1 MUX with active high output and active high enable
- **ONE** 1:4 DMUX with active high output and active high enable

Q5 Design a digital circuit that takes a digital signal of frequency F Hz as input and produces a digital signal of frequency (F/2) Hz as the output. Realize the circuit using minimum numbers of 2-input NAND gates only. [12]

Q6 Design a digital circuit with TWO 1-bit inputs (A and B), TWO 1-bit outputs (X and Y), and TWO select lines (P and Q). The circuit operates as explained in the table. Choose the required components from the list. [12]

P	Q	X	Y	Operation
0	0	SUM	Cout	Full adder
0	1	A=B	0	Comparator
1	0	0	AND	Logical AND
1	1	X-OR	0	Logical X-OR

List of components available
1. **One** Full Adder
2. **One** 1-bit Comparator
3. **Four** 4:1 MUX with active high enable and active high output.

Q7 Design a digital circuit that takes the BINARY number (ABCD; A: MSB and D: LSB) as input and produces its equivalent GRAY code (PQRS; P: MSB and S: LSB) as output. Realize the circuit using minimum numbers of half adders only. TRUE inputs are available for design. [12]

Q8 Obtain the minimum SOP form at output Y of the below circuit. [12]