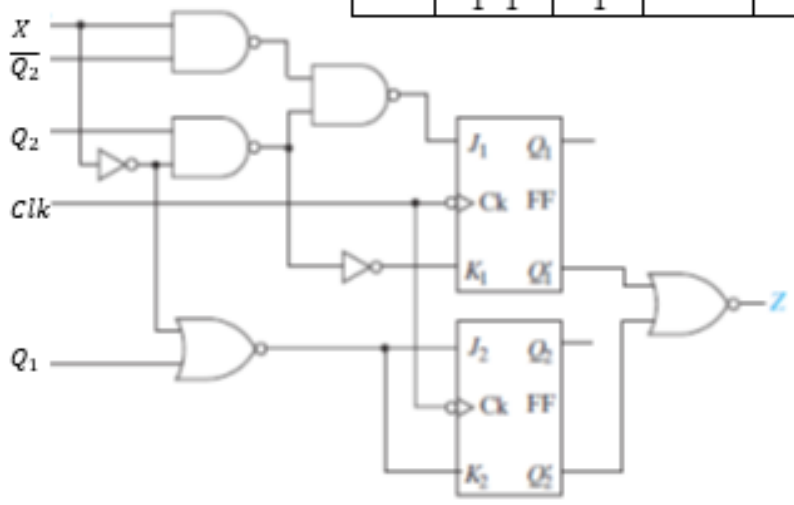
Birla Institute of Technology and Science, Pilani.
Comprehensive Examination: CS/ECE/EEE/INSTR F215: Digital Design
Marks: 40 AY: 2023-24, Semester: I Date: 18-December-2023, Monday
Time: 60 minutes CLOSED BOOK Pages:04

BITS ID:_____ **Name:**_____

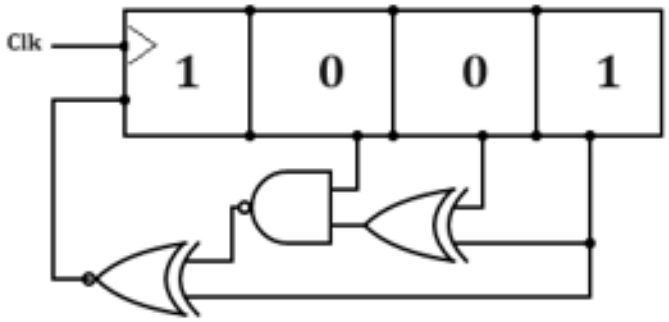
Q1 Realize the Boolean expression using the minimum number of Transmission Gates (TGs). $F(A,B,C,D) = \sum m(0,4,5,6,8,9) + d(10,11,12,13,14,15)$. True and compliment inputs are available. [5]

Q2 For the following sequential circuit, construct the state table. [5]

State	Present State $Q_2\ Q_1$	Input X	Output Z	Flip-flop Input		Next State $Q_2^+\ Q_1^+$
				$J_2\ K_2$	$J_1\ K_1$	
S_0	0 0	0				
	0 0	1				
S_1	0 1	0				
	0 1	1				
S_2	1 0	0				
	1 0	1				
S_3	1 1	0				
	1 1	1				



Q3 A 4-bit shift register is shown in the figure below. It is clocked, and with each clock pulse, the pattern gets shifted by a one-bit position to the right. [5]



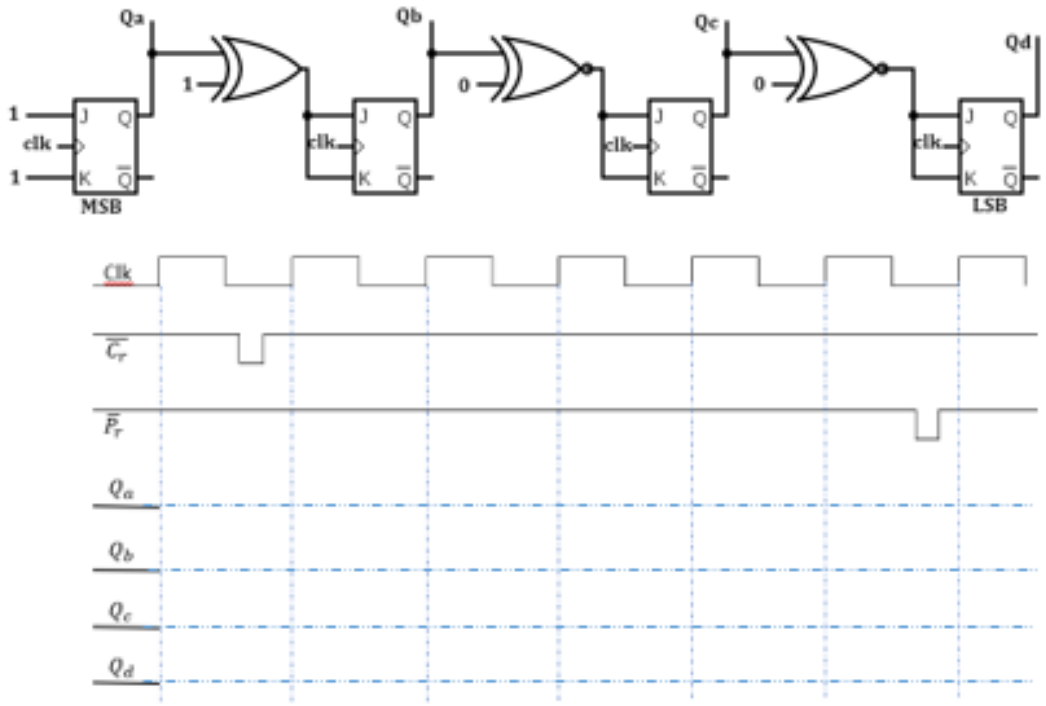
Assume that the initial value of the shift registers as 1001. Write the content of the shift registers after the following clock pulses:

	1	0	0	1
After 1st clock pulse				
After 3rd clock pulse				
After 5th clock pulse				
After 7th clock pulse				

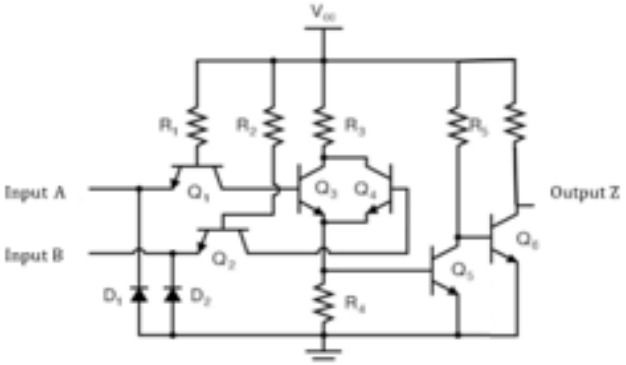
To what values should the shift register be initialized so that the pattern (1001) occurs after the first clock pulse:

Q4 Use the following table to perform the multiplication of two numbers, M (multiplicand) and Q (multiplier), using the booths algorithm. [5]
Assume $M = -12$ and $Q = 8$.

A	Q	Q_{-1}	Count	Command
00000	01000	0	-	Initialization

Q5	Draw the waveform corresponding to the circuit below; assume that preset and clear (both active low) of all the flipflops are commonly connected to "$\overline{P_r}$" and "$\overline{C_r}$" respectively. Clock is common to all flipflop.  	[5]
Q6	A full subtractor has three input (X, Y, Bin) and two output (D, Bout). Realize the Bout expression using minimum number of CMOS transistors. True and compliment inputs are available.	[5]

Q7 Identify the logic operation the given circuit performs on input A and input B. Also, complete the following table with respect to the state of the respective transistor (ON or OFF) for the various input combinations. [5]



An operation performed is:

Input A	Input B	Q3	Q4	Q5	Q6	Output Z
0	0					
0	1					
1	0					
1	1					

Q8 Complete the partial truth table for the given Verilog code: [5]

```
module Mini (
   input P, Q,
   output X, Y
);

assign X = P ^ Q;
assign Y = ~P & Q;

endmodule

module Top (
   input P, Q, R,
   output Q1, Q2
);

wire A, B, C;

Mini L0(P, Q, A, B);
Mini L1(A, R, Q1, C);

assign Q2 = B | C;

endmodule
```

P	Q	R	Q1	Q2
1	1	1		
0	0	1		
0	1	1		
1	0	0		
0	1	0		