BIRLA INSTITUTE OF TECHNOLOGY AND SCIENCE, PILANI
K.K BIRLA GOA CAMPUS
FIRST SEMESTER (2022-23) Comprehensive Examinations
Electronic Devices (EEE/ECE/INSTR F214)

Date: 21-12-2022 Time : 180 min Maximum Marks: 120 (40%) Closed Book

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Instructions: **(i) Answer All questions.**
(ii) Any required data not explicitly given, may be suitably assumed and stated.
(iii) All answers and figures should be written using PEN only.
(iv) Enclose the final answer in a box.

Q1. The Fig.1 shows the plot of steady state carrier concentrations inside a pn junction diode maintained at T=300K.
(a) Is the diode forward biased or reverse biased? Explain how you arrived at your answer.
(b) Do low level injection conditions prevail in the quasineutral regions of the diode? Explain how you arrived at your answer.
(c) Determine the applied voltage, V_A.
(d) Determine the hole diffusion length, L_P.
(e) What is p-side and n-side doping concentrations? **[12]**

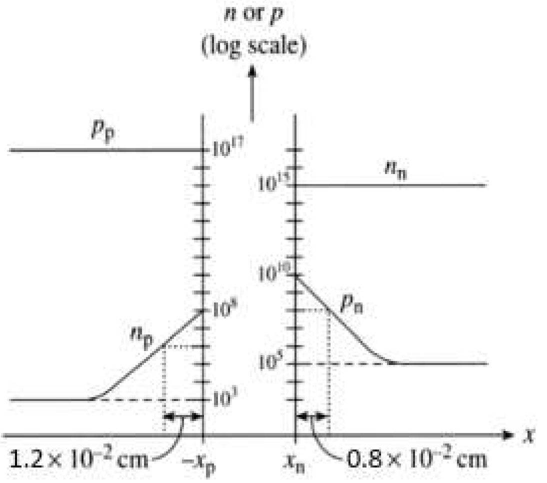

Fig.1

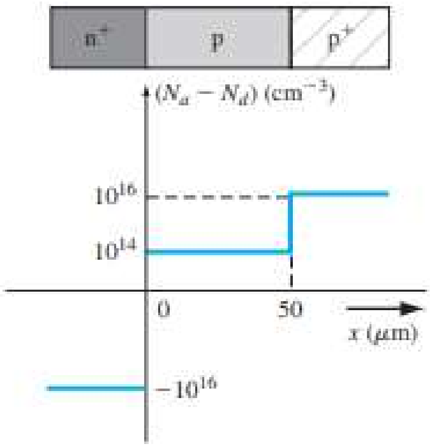

Fig.2

Q2. Consider a silicon pn junction with the doping profile shown in the Fig.2 at T=300K.
(a) Calculate the applied reverse bias voltage required so that the space charge region extends entirely through the p-region. (b) Determine the space charge width into the n+ region with the reverse bias voltage calculated in part(a). (c) Calculate the peak electric field for this applied voltage. **[12]**

Q3. (i) Assume that an MOS capacitor is designed with a p^+-polysilicon gate and a n-type silicon substrate of doping $10^{17}/cm^3$. (a) Draw the energy band diagram at zero applied voltages. (b) Determine the voltage required to achieve the flat band condition. (c) Identify the state of the MOS capacitor at zero applied voltage. (ii) In order to improve the performance of the MOS capacitor, an electrical engineer replaced SiO_2 (oxide layer) with Si_3N_4 (high dielectric material) with dielectric constant of 7.5. If the thickness of the Si_3N_4 is 4 nm, find the equivalent oxide thickness of the SiO_2. Assume the dielectric constant of SiO_2 is 3.9. Comment on the advantage of designing MOS capacitor with Si_3N_4. **[12]**

Q4. A Schottky diode with an n-type Si at T=300K yields the $1/C^2$ versus V_R plot shown in the fig.3, where C' is the capacitance per cm^2. Determine the (a) the built-in potential (b) the doping concentration (c) the barrier height. **[12]**

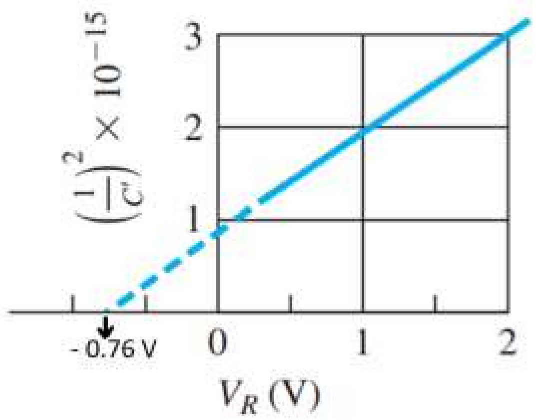

Fig. 3

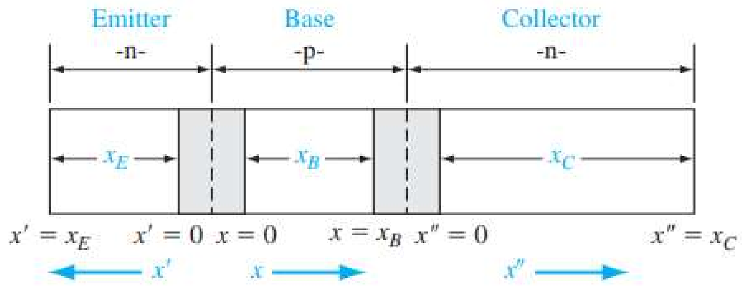

Fig.4

Q5. An enhancement type NMOS transistor with V_{TH}= 0.7 V has its source terminal grounded and a 1.5V dc applied to the gate. In what region does the device operate for (a) V_D = 0.5 V (b) V_D = 0.9 V (c) V_D = 3 V. Give proper justification for the answers. If the transistor has $\mu_n C_{ox}$ = 100 μA/V^2, W= 10 μm and L= 2 μm, find the value of drain current in each case. **[12]**

Q6. An enhancement type NMOS transistor with V_{TH} = 0.7 V conducts a current I_D= 100 μA when V_{GS} =V_{DS} = 1.2V. Find the value of I_D for V_{GS} = 1.5V and V_{DS} = 3V. Also calculate the value of the drain-to-source resistance r_{DS} for small V_{DS} and V_{GS} = 3.2V. **[12]**

Q7. An NMOS transistor is fabricated in a 0.4 μm process having $\mu_n C_{ox}$= 200 μA/V^2 and V_A= 50V/μm of channel length. If L=0.8 μm and W= 16 μm, find the value of λ. Find the value of I_D that results when the device is operated with an overdrive voltage of 0.5V and V_{DS}= 1V. Also find the value of r_0 at this operating point. If V_{DS} is increased by 2V, what is the corresponding change in I_D? **[12]**

Q8. The PMOS transistor shown in Fig.5 has V_{TH} = – 1.0 V, $\mu_p C_{ox}$= 80 μA/V^2 and W/L= 12.

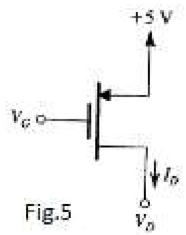

Fig.5

(a) Find the range of V_G for which transistor conducts.
(b) In terms of V_G, find the range of V_D for which the transistor operates in the triode region.
(c) In terms of V_G, find the range of V_D for which the transistor operates in the saturation region.
(d) Neglecting the channel length modulation, find the values of overdrive voltage and V_G and the corresponding range of V_D to operate the transistor in the saturation mode with |I_D |= 75 μA.
(e) If λ= 0.02 V^{-1}, find the value of r_0 corresponding to the overdrive voltage determined in (d). **[12]**

Q9. The measured drain currents for a given n-channel Si MOSFET(with substrate connected to source) with N_A=10^{16}cm^{-3}, VDS=3 V, t_{ox} = 65 nm , W = 10 μm and L= 2.0 μm are as follows:

V_G = 1 V	V_G = 2V
I_D=87 μA	I_D=136 μA

(a) Determine the threshold voltage and effective mobility of charge carrier for the NMOS transistor.
(b) Now the substrate is biased such that V_{SB}= 2 V. Find the change in the threshold voltage. **[12]**

Q10. A uniformly doped silicon npn bipolar transistor at T = 300 K shown in Fig.4 is biased in the forward-active mode with the B-C junction reverse biased by 3V. The metallurgical base width is x_{B0}= 1.0 μm. The doping concentrations are N_E = 10^{17} cm-3, N_B=10^{16} cm^{-3} and N_C= 10^{15} cm^{-3}.
(a) At T=300K, calculate the base emitter voltage at which the minority carrier electron concentration at x=0 is 10 percent of the majority carrier hole concentration. (b) at this bias, determine the minority carrier hole concentration at x'=0 (c) determine the neutral base width for this bias. **[12]**

List of constants:

k= 8.62 × 10^{-5} eV/K At T=300K kT=0.0259 eV q= 1.6 × 10^{-19} C n_i (Si) = 1.5 × 10^{10} cm^{-3}
ε_o=8.854 × 10^{-14} F/cm ε (Si) = 11.8 ε_o μ_p (Si) = 480 cm^2/V-s N_c(Si)= 2.8 × 10^{19} cm^{-3}
μ_n (Si) = 1350 cm^2/V-s ε(SiO_2) = 3.9 ε_o E_g(Si) = 1.1 eV χ(Si)= 4.01 eV N_V(Si) = 1.04× 10^{19} cm^{-3}