# Birla Institute of Technology and Science Pilani , Rajasthan

**Ist semester 2016-2017**

**EEE F214/ INSTR F214 (Electronic Devices )**

**Comprehensive Examination [Part A(closed Book) + Part B (Open Book)]**

**Part B (Open Book)**

**Date: 07/12/2016** **MM : 80** **Time:120 min**

Note: Use following data if not given in a problem.

**$\varepsilon_o$ = $8.86\times10^{-14}$F/cm, $\varepsilon_r$ ($SiO_2$) = 3.9, $\varepsilon_r$ (Si) =11.8, At room temperature for Si [$N_C=2.8\times10^{19}$ /$cm^3$, $N_V=1.04\times10^{19}$ /$cm^3$, $\mu_n=1350 cm^2/V\cdot S$, $\mu_p=480$ $cm^2/V\cdot S$, $n_i=1.5x10^{10}/cm^3$ ,$q\chi=4.05$ eV, $E_g=1.12$eV], for Ge [$n_i=2.4x10^{13}$ /$cm^3$ ,$q\chi=4.13$ eV, $E_g=0.66$ eV], for GaAs [$n_i=1.8x10^6$ /$cm^3$ ,$q\chi=4.07$ eV, $E_g=1.42$ eV] k =$1.38\times10^{-23}$ $m^2$ Kg $s^{-2}$ $K^{-1}$, $\tau_n=\tau_p=1\mu s$, kT/q = 0.026V.**

**1.(a):** Sketch and label CV plot for an n-substrate MOS capacitor having 1.5 x $10^{15}$ dopants /$cm^3$ with 10nm thick $SiO_2$ for the following cases:

(i) for an applied 10KHz input signal.

(ii) for a slow voltage ramp signal applied at the gate. **[10]**

**(b):** Find the $V_T$ of a p-substrate MOS structure having 10nm $SiO_2$ thickness ( $t_{ox}$ ) and $n^+$ poly Si gate where the change in flat band voltage $V_F$ is found as 0.1V when the oxide layer thickness is changed from 10 nm to 15nm. Sketch and label energy band diagram for this MOS ($t_{ox}$ =10nm and substrate doping of $10^{16}$ /$cm^3$). Further, extend the sketch if on the other side of semiconductor an $n^+$ poly silicon layer is also grown. **[10]**

**2. (a):** Derive an expression for the ratio of diffusion and drift currents in an n-MOS transistor under strong inversion case at lower $V_D$. Comment on the contribution of these on the total current of the device. **[8]**

**(b):** For silicon based device there are three regions, region-1 doped with $1.5x10^{16}$ donors/$cm^3$, region-II is un-doped and region-III is acceptor doped with $6x10^{16}$/$cm^3$. The depletion region thickness in region-1 is 100nm and the un-doped region is also kept as 100nm. Sketch and label electric field profile across the p-n junction and also compute the junction capacitance in unbiased case. Find the built in potential across the junction. Which region will limit the possible reverse bias for proper operation if the physical thicknesses of both the p and n regions are kept as 300nm, comments with reason? (Assume region II extend from $x \geq 0$)

**[12]**

**3. (a):** In a pnp transistor the current $I_{EP}$ in base region is given by

$$I_{EP}= qAp(x_n)\, E \; - qAD_p\, dp(x_n)/dx_n$$

Show that $I_{EP}$ can also be expressed by the following formula

$$I_{EP}= -(qAD_P/n)\, .\, d(p.n)/dx$$

Now, reduce this expression for $I_C$ under the low level injection in terms of excess hole carriers at EB-junction under appropriate condition. **[8]**

**[P.T.O]**

**(b):** Derive an expression for photo current ( $i_{ph}$ ) in terms of incident optical power $P_{in}$ having photo wavelength as $\lambda$. Sketch and label the detector responsivity R(= $i_{ph}/P_{in}$) with respect to $\lambda$, both for a theoretical and practical Si based detector . In the given detector circuit shown in Fig 1, find the diode power dissipation for a 10mW input light and estimate the limit of maximum incident power in the detector. (Assume all incident light is converted into current and R as 0.4A/W)

**[12]**

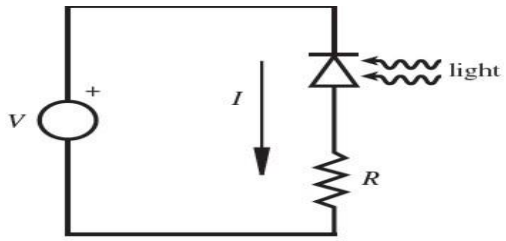


Fig 1.

**4. (a):** A Si sample with an area of cross-section $10^{-4}$ $cm^2$ shows a Hall-Coefficient $R_H$ = +41.7 $cm^3/C$ and a junction potential as 0.718V at room temperature (300 K). Sketch and label the following:

(i) Energy band diagram across p-n region

(ii) Electric field across junction

(iii) Current through a diode for a forward bias of 0.6V

(iv) Current distribution (diffusion/drift) across p-n junction starting from one end of the metallic junction to the other end of metallic junction **[12]**

**(b):** In the following figures, the energy band diagram of a semiconductor structure is shown.

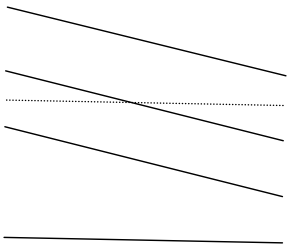

**Fig 2(a) .** Silicon at room T

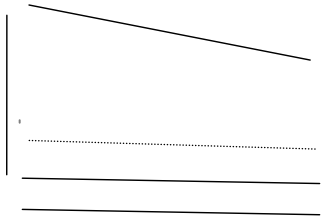

**Fig 2(b).** A doped semiconductor

Sketch and label

1. Electric field for both the cases with respect to x.
2. Minority carrier distribution with respect to x (only qualitatively) **[8]**

----------****----------****----------