Birla Institute of Technology and Science, Pilani
ECE/EEE F244 / INSTR F244 Microelectronic Circuits
Mid-semester Test, II Semester 2022-2023
CLOSED BOOK

Time: 90 min.	Max. Marks = 80	Date: 13-3-2022 (9-10:30 am)

Unless given specifically
Take -- V_{DD} / Vcc = 4 V,
For NMOS device $\mu_n Cox$ = 140 μA/V², V_{Tn} = 0.7 V, λ= 0.1 V⁻¹, γ= 0.45 √V, Cox= 0.38pF/μm²
For PMOS device $\mu_p Cox$ = 40 μA/V², V_{Tp} = - 0.8 V, λ= 0.1 V⁻¹, γ= 0.4 √V, Cox =0.38 pF/μm²
For NPN/ PNP β =100, $|V_{BE}|$= 0.7 V, and V_t =25 mV, α=1, $I_S = 10^{-12}$A, V_A =100V, Vce,sat = 0.2V

NOTE:

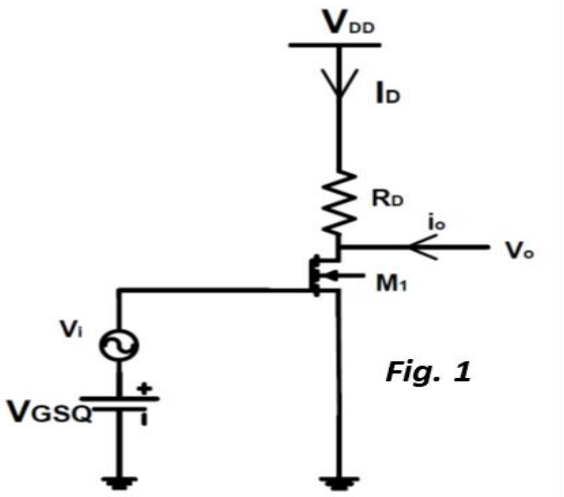
If not specified in the question, ------

- Ignore γ, λ in the drain current equation. Assume matched components wherever required
- Specify your assumptions. Justify your answers. Unless specified, assume all MOSFETs are biased in the saturation region. Label your sketches properly. All symbols have usual meaning.
- The body (B) terminals of all the PMOSFETs are connected to V_{DD}, NMOSFETs are connected to the ground.

Q1. (a) Consider the Circuit shown in **Fig. 1**.

V_{DD} = 5 V, R_D = 5 kΩ, V_{GSQ} = 2 V, $\mu_n Cox$ (W/L) = 0.5 mA/V², V_{tn} = 0.8 V, λ ≈ 0.

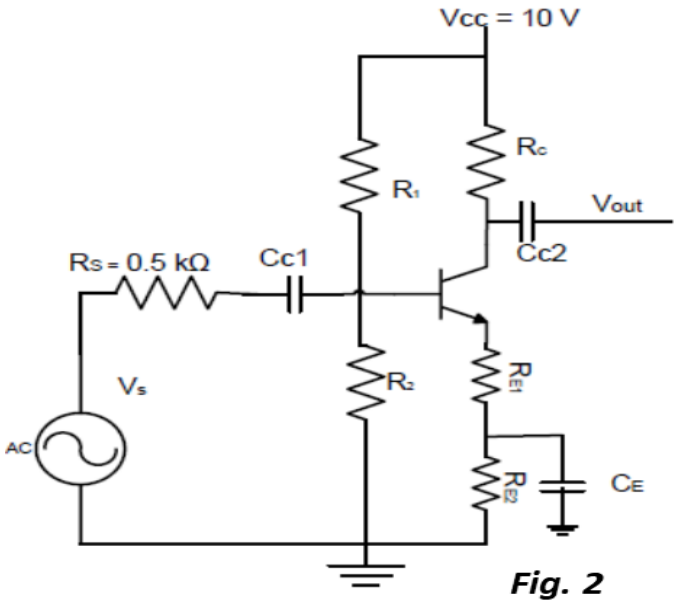
I. Calculate the quiescent values $\mathbf{I_{DQ}}$ and $\mathbf{V_{DSQ}}$.
II. Determine the low-frequency small signal voltage gain $(\mathbf{v_o/v_i})$.
III. If $v_i = 0.1 \sin \omega t$ V, sketch and label the $\mathbf{i_o}$ and $\mathbf{V_o}$ waveforms properly with respect to time.



Q1. (b) For the circuit given below in **Fig. 2:**

β = 100, R_1 = 200 kΩ, R_2 = 200 kΩ, R_{E1} = 240 Ω, R_{E2} = 20 kΩ, R_C = 2kΩ, $V_{BE(ON)}$ = 0.7 V, V_A = ∞, $V_{Thermal}$ = 0.025V

I. Identify the circuit topology.
II. Calculate the $\mathbf{I_{CQ}}$ and $\mathbf{V_{CEQ}}$.
III. Find small signal parameters $\mathbf{g_m}$ and $\mathbf{r_\pi}$.
IV. Draw and label the small signal model and calculate the low-frequency voltage gain $(\mathbf{V_{out}/V_s})$.
V. How will the $\mathbf{I_{CQ}}$ change for the given circuit if the value of $\mathbf{R_{E1} = R_{E2} = 0}$ in the circuit? Comment on the operating region of the amplifier after the above change.



[22 Marks]

Q2. Consider the 2-port network representation of a unilateral system shown in **Fig. 3**.

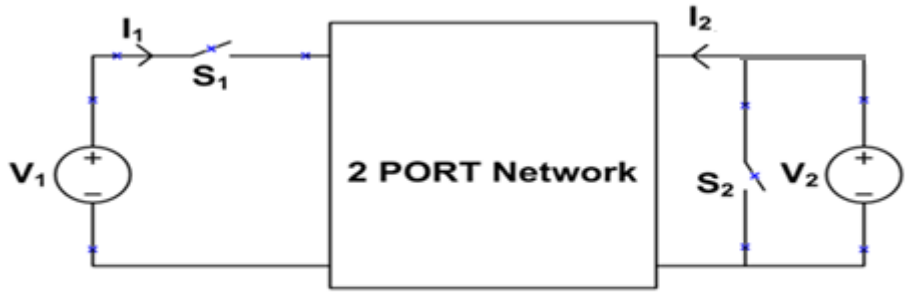


Fig. 3

Given ----

- **When S_1 closed and S_2 closed: V_1 = 0.5V, I_1 = 10µA and I_2 = 1mA**
- **When S_1 open and S_2 open: I_2 = 1mA and V_2 = 5V.**

I. Find the **h-parameter** matrix. Also, Sketch and label the **h-parameter** model of the network.

II. Find the **z-parameter** matrix. Also, sketch and label the **z-parameter** model of the network.

III. If a signal source $\mathbf{V_i}$ **= 0.5V** is connected to port 1 of the **z-parameter** model and a load resistance of **25kΩ** is connected to port 2 of the model. Now, calculate the following in **dB;** voltage gain ($\mathbf{V_{out}/V_i}$), current gain ($\mathbf{I_o/I_i}$) and Power gain.

[18 Marks]

Q3. Consider the circuit of **Fig. 4**. Ignore the body bias effect (Perform intuitive analysis)

Given: **MOSFET: λ=0.1V^{-1}, V_{tn}=1V, $\mu_n C_{ox}$ = 100µA/V^2, V_{ov} = 0.2V**

BJT: V_{BEon} = 0.6V, V_A= 100V and V_{CEsat} = 0.2V

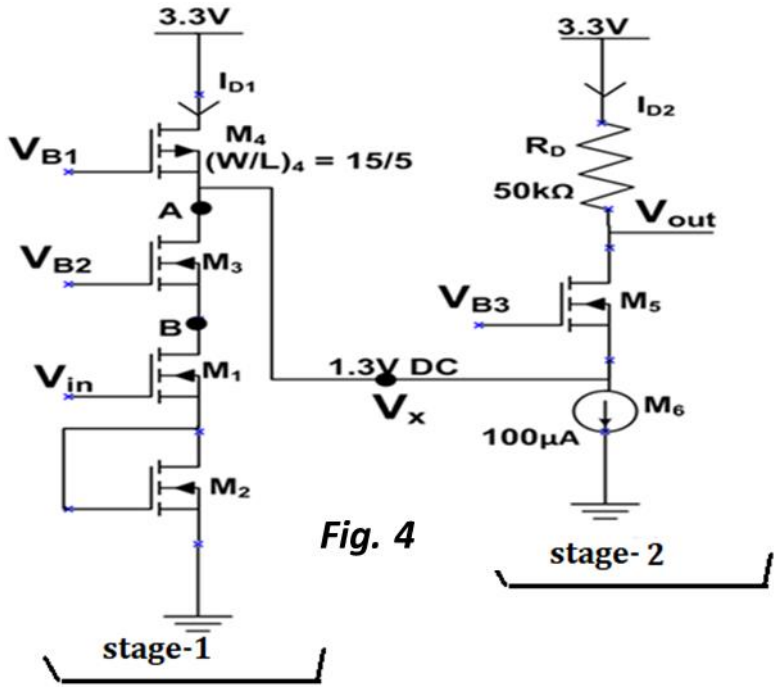


Fig. 4

I. Identify the topology of **stage 1** and **stage 2.**

II. Calculate the current $\mathbf{I_{D1}}$.

III. Calculate the voltage swing at nodes $\mathbf{V_x}$ and $\mathbf{V_{out}}$.

IV. Sketch and label the **small signal model.**

V. Calculate the $\mathbf{G_m}$ and $\mathbf{R_{out}}$ of **Stage-1.** Hence, find the gain $\mathbf{V_x/V_{in}}$ and $\mathbf{V_{out}/V_x}$. (Hint: Consider loading effect of stage 2 in calculations)

VI. Assume, node $\mathbf{V_x}$ **is connected to node B**. Now, calculate $\mathbf{G_m}$ and $\mathbf{R_{out}}$ of **first** stage (Hint: Consider loading effect of stage 2 in calculations) **[25 Marks]**

Q4. Circuit shown in **Fig. 5(a)** is used to bias circuit shown in **Fig. 5(b),** and generate voltages $\mathbf{V_{B1}}$, $\mathbf{V_{B2}}$, $\mathbf{V_{B3}}$, using MOSFET transistors. Assume all the transistors are operating in active region.

- Given that the total power consumption of **Fig 5(a) and Fig. 5(b)** together is **7500 µW**
- Assume $\mathbf{|V_T|= 1V}$, $\mathbf{V_{ov}=0.2V}$ for all the transistors.

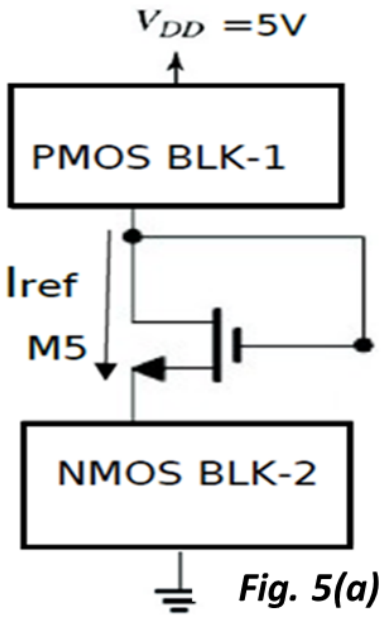


Fig. 5(a)

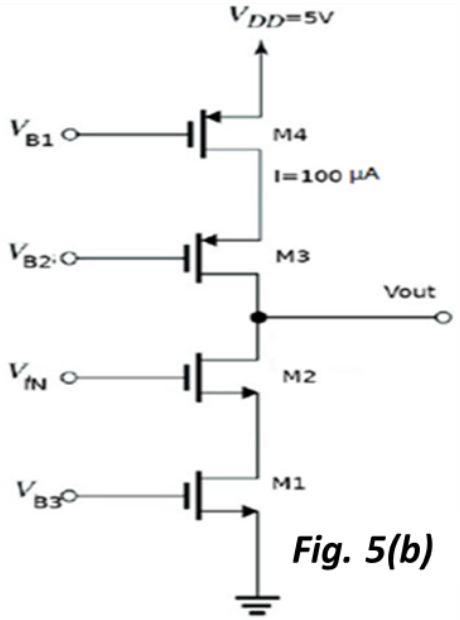


Fig. 5(b)

I. Determine the value of $\mathbf{I_{REF}}$ current.

II. Now, sketch the schematic of **NMOS block (BLK2) in Fig. 5(a).**

III. Draw the circuit (schematic) of **PMOS block (BLK1) in Fig. 5(a)**. Hence, draw the complete circuit of **Fig. 5(b)** including biasing circuit.

IV. Now, for **Fig. 5(b),** compute **DC** values of voltages $\mathbf{V_{B1}}$, $\mathbf{V_{B2}}$ **and** $\mathbf{V_{B3}}$

V. Determine the value of $\mathbf{V_{GS}}$ of transistor **M5** shown in **Fig. 5(a).** **[15 Marks]**

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