Birla Institute of Technology and Science, Pilani
ECE/EEE / INSTR F244 F244 Microelectronic Circuits
Comprehensive Examination, II Semester , 2022-2023

Note----(Specify your assumptions clearly.)

Unless given specifically
Take -- $V_{DD} = V_{CC} = 3.3V$,
For NMOS device $\mu_n Cox = 140\ \mu A/V^2$, $V_T = 0.7$ V, $\lambda = 0.1\ V^{-1}$, Vov=0.2 V
For PMOS device $\mu_p Cox = 40\ \mu A/V^2$, $V_T = -0.7$ V, $\lambda = 0.1\ V^{-1}$, Vov=0.2 V
For NPN/ PNP device β=100 V, $V_{CE,SAT}$ =0.2V , V_A=100V, kT/q= 25mV(at room temp.), Is= 10^{-14} A, $V_{BE,ON}$ = 0.6V, α≈1
NOTE:
If not specified in question ------
- Ignore γ, λ in drain current equation. Bulk of nmos connected to ground and bulk of pmos connected to V_{dd}.
- Unless specified, assume all MOSFETs are biased in the active region All symbols have the usual meaning.

Part A: CLOSED BOOK *Total **2** questions in Part A.*

Time: 60 minutes **Max. Marks=40** **Date: 06-05-2023**

Answer all the sub-parts of a question in sequence and one place only. Clearly show the procedure used to arrive at the answer for full credit. Report the answers with proper units.

Q 1. Consider the Amplifier circuit given in **Fig.1**. Following values are given for the circuit: R_F = 100 KΩ, R_D = 5 KΩ, R_L = 5 KΩ, K_n' = 20 μA/V², L = 10 μm, W = 200 μm, V_A = 100 V, V_t = 2 V. Assume all the capacitors are open for DC bias and short at given signal frequency.

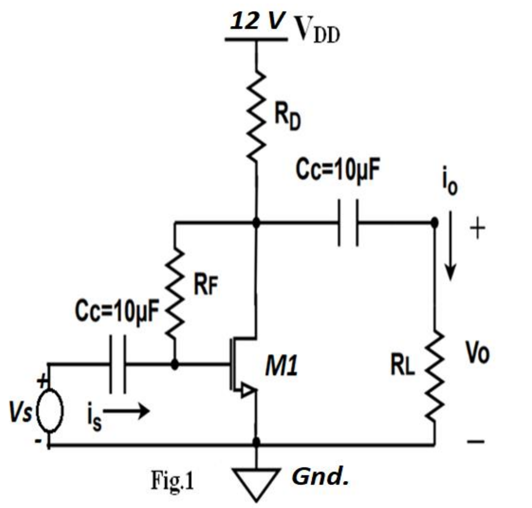

Fig.1

Determine the following:
a) DC Operating point $(I_{DQ}, V_{GSQ,} V_{DSQ})$
b) Input Impedance and Output Impedance
c) Voltage gain and Current gain

[20 marks]

Q 2. ***(A)*** Consider the circuit of **Fig. 2**

Given, $|V_{tn}| = |V_{tp}| = 0.6V$, $\mu_n C_{ox} = 200\ \mu A/V^2$, $\mu_p C_{ox} = 60\ \mu A/V^2$.
---The channel length of all transistors=1 μm.
----The minimum allowed drain voltage at M_1 and M_4 are -1.3V and 1.3V, respectively.

Find the widths of M_1, M_2, M_4.

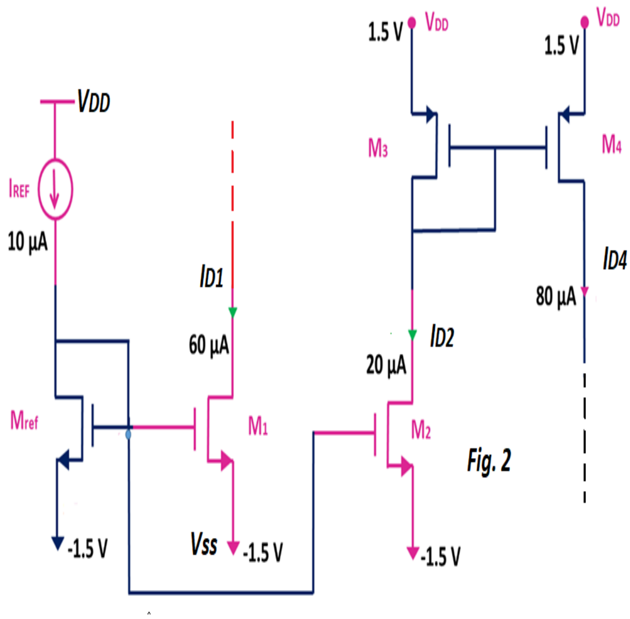

Fig. 2

Q2(B) For a p-channel long MOSFET, threshold Voltage (V_T) = -1 V, W = 20 μm, L = 2 μm. Given, μ_p = 200 cm²/V-s, C_{ox} = 3.5 × 10^{-7} F/cm². The source and body are connected to the ground.

Calculate the drain current for following conditions----

a) at V_G = -4 V, V_D = -1 V.
b) at V_G = -3 V, V_D = -3 V.

[20 marks]

--------------------------**End of Part-A**------------------------

BITS Pilani EEE/INSTR/ ECE F244 Microelectronic Circuits
Second Semester 2022-23

Time: 2 hrs. **Comprehensive Exam (Open Book)** **Total Marks: 70**

Part-B (Open Book)

Use data/parameters given in part (A)

NOTE-- There are **FOUR** questions. Answer all the sub-parts of a question in sequence and one place only. Clearly show the procedure used to arrive at the answer for full credit. Report the answers with proper units.

Q1. Consider the circuit shown in Fig 1., where the applied input voltages are:

vin_1 =5mv sinwt +1.4V *and* ***vin_2 =10mv sinwt +1.4V*** .

--Transistors M1, M2 has **Vov= 0.2 V.** The value of **Iss=90 uA**

-- Iss is implemented with basic current mirror with **large Rss**.

--Assume perfect matching of transistors,

--Resistors with **R_{D1} = R_{D2}= R_D=40 KΩ** .

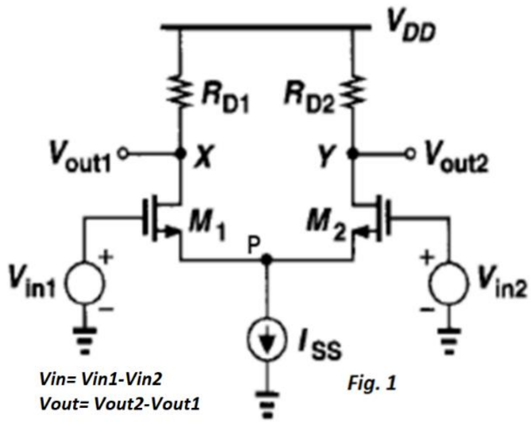

Fig. 1

a) Now, analyze the given circuit and calculate the dc voltage at **nodes P and X.**

b) Calculate the differential mode gain , **(Adm),** for the given circuit.

c) Determine common mode component of each input signal (vin1 and vin2) and differential mode component of each input signal (vin1 and vin2)

d) Now, determine a.c value of total **Vout** tapped between vout1 & vout2 nodes. (Vout = vout1-vout2).

e) Finally, draw a **labelled plot** for Vout (t) vs. time. (show both DC and AC components)

[19 marks]

Q2. **(A)** Consider **Fig 2a**

Given: **W/L= 25, R_1 ll R_2 = 100kΩ, V_{TN} = 1V, I_{DQ} = 2mA, R_D = 2.5kΩ, Vdd=12 V**

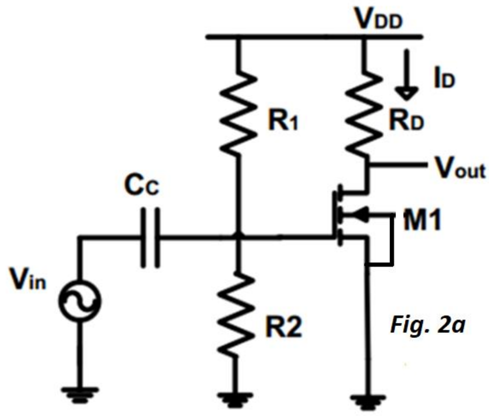

Fig. 2a

a) Draw the Load line of the given circuit and mark the maximum value of I_D and V_{DS} on the x-axis and y-axis, respectively.

b) Find the value of V_{DSQ} and V_{GSQ} in such a way that the Q point is in the **middle** of the saturation (active) region.

c) Find the value of R_1 and R_2.

Q2 (B) Consider **Fig. 2b of** cascode amplifier, **Vdd/ Vcc=12 V**

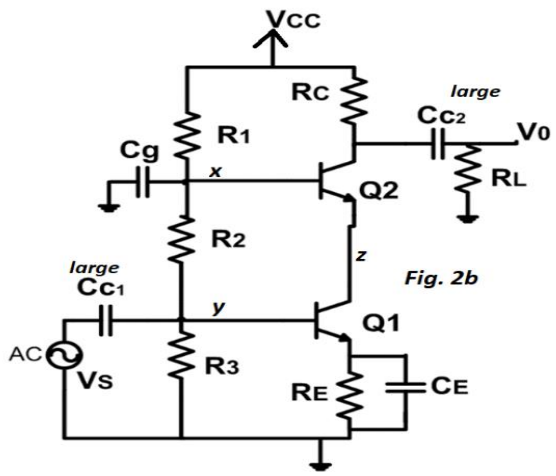

Fig. 2b

d) Sketch and label the small-signal (low frequency) equivalent model for the given amplifier. **(Assuming λ⇒ 0)**

e) Find out the gain expression of the above amplifier. Compare the gain expression with a conventional Common emitter/base amplifier.

[Total 19 marks]

Q3. Consider the circuit given below in **Fig. 3**.

The Following parameters are given:

$\mathbf{V_{ov} = 0.2V, \lambda = 0.01V^{-1}, \quad C_{gs(1,2)} = 10pF,}$

$\mathbf{C_{gd(1,2)} = 1pF, C_{db(1,2)}=2pF, C_{sb(1,2)} = 2pF}$ **and**

$\mathbf{R_s << 1/g_m}$

Ignore the capacitances of the basic current mirror current source M3

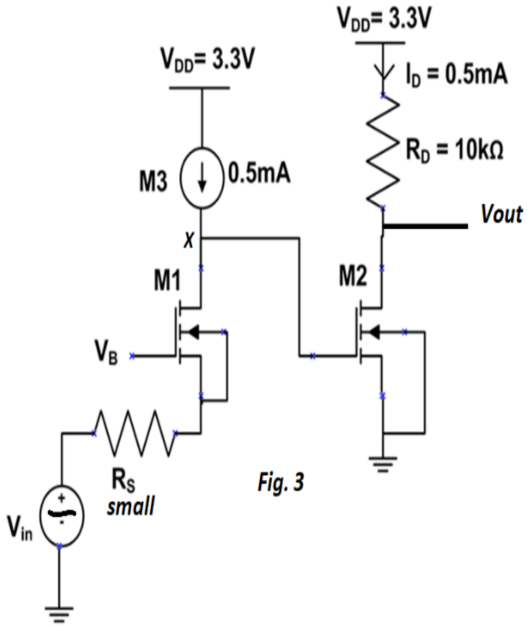

Fig. 3

a) Sketch and label the high frequency model of the amplifier.

b) Identify the **number of** dominant poles and zeros of the amplifier.

c) **Calculate** the frequency (in rad./s) of the **dominant poles and zeros** of the amplifier.

d) Calculate the **phase** of the amplifier at **ω= 10K rad/s.**

e) Plot and label the **Bode magnitude response** of the amplifier (Use corner plot) qualitatively. Mark the values of low frequency voltage gain (**vout/vin**) and the dominant poles and zeros along with UGB on it.

f) Calculate the unity gain frequency (**UGB in rad./s**)

[17 marks]

Q4. Consider the circuit given in **Fig. 4**.

The bias current I5= 25uA , Iss=200 uA.

For all devices take, V(overdrive)= 0.2 V ,

λ=0.01 V^{-1} Assume load capacitance at output is

C_L= 1nF , Rsig is small

R_p= 1KΩ, R_F= 1MΩ, R_S= 1KΩ

Neglect body effect in calculations.

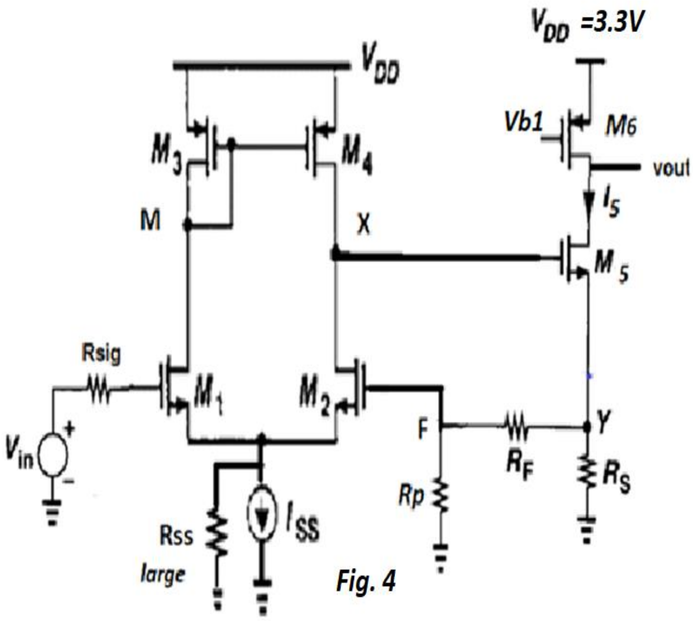

Fig. 4

a) Identify the **type of feedback** in this amplifier. Hence determine **type** of input and output signal of feedback amplifier

b) Determine the **open loop** parameters A_o, R_{out} at low frequency

c) Determine **closed loop** parameters: A_{0f}, R_{inf}, R_{outf} , feedback factor (β) at low frequency

d) Assuming that **output node pole** is dominant pole, determine the **-3dB frequency**, and **UGB** (unity gain bandwidth) in both **open loop** and **closed loop** condition.

Also determine **gain-crossover frequency** (Gx) in closed loop mode.

(15 marks)

***** End of Part-B *****