Birla Institute of Technology and Science Pilani (Rajasthan)
Department of Electronics and Electrical Engineering
Analog Digital VLSI Design (EEE/INSTR F313)
First Semester 2016-17

A

Date : 05/12/2016 **COMPREHENSIVE EXAM** **Max. Time: 3 HRS.**
Time: 09:00 AM to 12:00 PM **(Section-A Closed Book)** **Max.Marks:100**
(60 minutes, 30 Marks)

Name_____ **ID No.** | | | | | | | | | | | | | |

Instructions to the candidate

Please write your answers legibly and neatly in the ***separate answer Sheet provided*** *only.*
Crossed Answers *shall not be considered for a recheck.*
There is ***no partial marking*** *in this part of the exam.*
All questions are compulsory and carry ***3.0 marks*** *each.* ***No Negative marking****.*
You may use the ***supplementary answer sheet*** *for rough work which* ***will not be considered for evaluation****.*

Common data for PART-A*: Use the following data if not mentioned specifically in the question.*
$V_{DD} = 3V$, $|V_{TOP}| = 0.8V, V_{TON} = 0.6V$, $KP_P = \mu C_{ox} = 50\,\mu A/V^2, KP_N = 150\mu A/V^2$, $C_L = 100fF$, $f = 850MHz$, $L_{min}\,(2\lambda) = 0.3\mu m$.

Each question carries ***THREE*** *marks. Write your answers in the separate answer sheet provided.*

1. Assuming minimum length transistors calculate the ratio of width of PMOS and NMOS in a static CMOS inverter that produces an output voltage of 2.2V for an input voltage of 1.2V.

2. In static CMOS logic family if the rise time and fall time of the input signal increases, then which component of the power consumption changes and why? (Max. 3 sentences)

3. Justify the statement *"The switching power consumption at the output node of a pass transistor logic is low in comparison to static CMOS family"*. (Max. 3 sentences)

4. If a design engineer wants to selectively eliminate the body effect for PMOS in a given circuit, what exactly does he/she mean from the fabrication perspective. (Max. 3 sentences)

5. Is it possible to reduce the delay of a critical path, hence the overall circuit delay by modifying the threshold voltage of the MOSFETs on the critical path? If so, how? (Max. 3 sentences)

6. For the arrangement shown in **fig.1** (Note: *cd-contamination delay, pd-propagation delay and su-setup time)*. Calculate the maximum clock frequency if the positive skew 25ps.

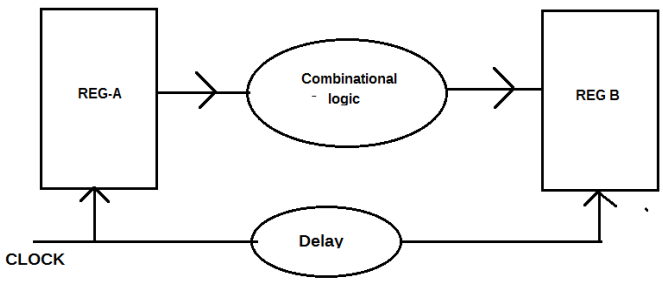

Figure 1: Question no.6

$T_{cd\text{-}Logic} = 25$ ps	$T_{pd\text{-}cq\text{-}B} = 25$ ps
$T_{pd\text{-}cq\text{-}A} = 25$ ps	$T_{cd\text{-}cq\text{-}B} = 15$ ps
$T_{cd\text{-}cq\text{-}A} = 10$ ps	$T_{su\text{-}B} = 12$ ps
$T_{su\text{-}A} = 12$ ps	$T_{hold\text{-}B} = 15$ ps
$T_{hold\text{-}A} = 10$ ps	$T_{pd\text{-}Logic} = 50$ ps

7. Logic families in List-A and the properties of them are randomly listed in List-B. Match all the properties a logic family obeys (Report the appropriate alphabet)

S.No.	List-A (logic family)			List-B (property)
i.	DCVSL	**[_____]**	**[a]**	Rail to Rail Swing
ii.	Pseudo NMOS	**[_____]**	**[b]**	Zero Static Power Consumption
iii.	Transmission Gate	**[_____]**	**[c]**	Ratioed logic
			[d]	Dynamic logic

8. Calculate the current Iout from **fig.2.** (neglect channel length modulation)

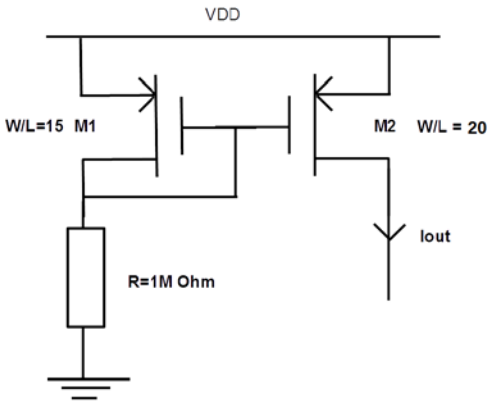

Fig.2. Question 8

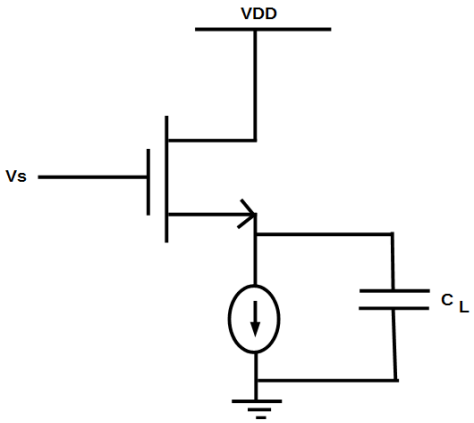

Fig.3. Question 9

9. For the source follower circuit shown in **fig.3.** Write the expressions for pole/s and zero/s If any? (neglect body effect)

10. Write an expression for positive and negative slew rate (C1 and C2 dominate over parasitic capacitances) for the single ended Op-Amp shown in **fig.4.**

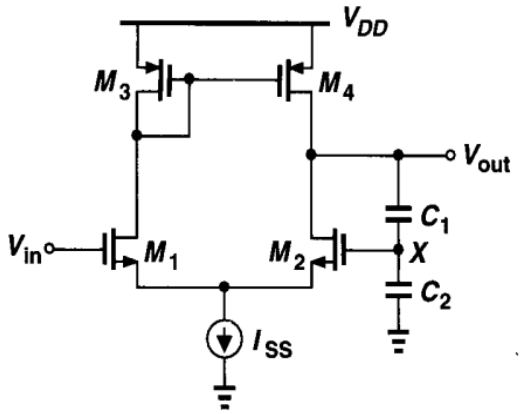

Fig.4. Question 10

*****All The Best*****

B

Section-B (OPEN BOOK) (70 MARKS)

General Instructions to the candidate

- *Please write your answers legibly and neatly. Answer **section-A and B** in **separate** answer booklets/ sheets provided.*
- *Symbols, constants, terminology used have their usual meaning unless specified specially.*
- *There are a total of **FIVE** (analog design-sectionB) questions and all are compulsory. Each carries marks as indicated.*
- *Answer the **sub-parts** of a question at one place and in the order in which they appear.*
- *Preferably start each question on a **fresh page** however, sub parts can be written in continuation.*

***Common data**: Use the following common data if not mentioned specifically in the question*

For 0.5µm Technology node $V_{DD} = 3.3V$, $V_{Thermal} = 26mV$

- *Use long channel approximation and lambda based design rules unless specially mentioned.*
- *Assume matching of transistors where ever required.*
- *Assume all transistors operating in saturation region unless specified*
- *Use square law current equation unless specifically mentioned.*
- *Neglect body effect, channel length modulation if not mentioned specifically.*
- *The body of all PMOS is tied to V_{DD} while all NMOS is tied to ground unless specially mentioned.*
- *Rough work should be crossed properly.*

	V_{T0} (V)	μc_{ox} ($\mu A/V^2$)	λ (V^{-1})	L_{min} (µm)
NMOS	0.7	140	0.1	1
PMOS	-0.8	40	0.1	1

Q1 For the voltage reference circuit shown in Fig. Q1 , $AE_{(Q1)} : AE_{(Q2)}$ = 10: 1, where AE is the emitter area of transistor. Transistor M1, M2, M3 are perfectly matched and have equal W/L ratio.

Given at room temperature V_{EB2} = 0.7V, $V_{thermal}$= 26mV,

$\frac{\partial v_{BE}}{\partial T} \approx -1.91 \frac{mV}{o_K}$ $\frac{\partial V_{thermal}}{\partial T} \approx +0.087 \frac{mV}{^oK}$

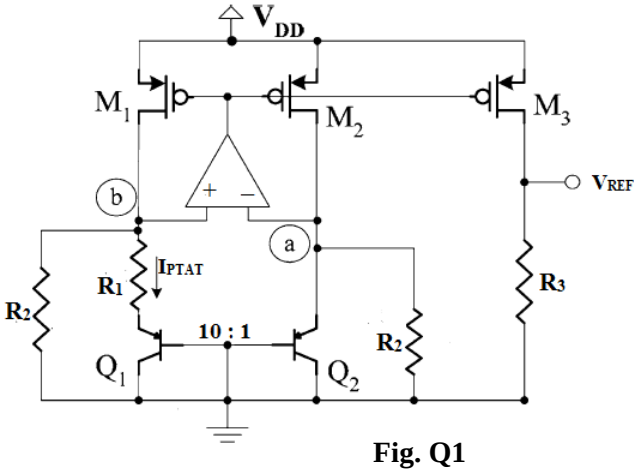

Fig. Q1

(i). Write the expression for V_{REF}.

(ii). Now find out the value of (R_2/R_1) to obtain zero T_{CF} at room temperature, Ignore the T_{CF} of resistors.

(iii). Find out the value of R_3 for V_{REF} = 0.67V at room temperature, if R_1 is assumed to be 2 kΩ.

[13M]

Q2 For the circuit shown in fig. Q2. Assume output load capacitances of 2pF, power consumption of 93µW and matching of transistors wherever required. Take V_{ov} = 0.2V for all transistors. Iss is basic current mirror circuit.

(i). Identify the circuit and calculate ICMR and OCMR.

(ii). Determine output signal swing.

(iii). Also, calculate the value of voltage gain (vout/ vin) and slew rate.

(iv). Redraw, the circuit for single ended output where transistor (M5-M8) should be configured as a low voltage cascade.

(v). Now, recalculate ICMR/OCMR of circuit of part (iv) in unity gain feedback mode.

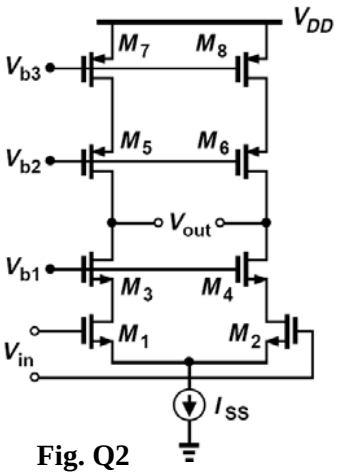

Fig. Q2

[14M]

Q3 For Fig Q3, assume current source symbol Iss is represented by a low voltge cascode current mirror. Vin= vin1-vin2, Vout=vout1-vout2,

Given, all transistors have equal Vov (overdrive volage)= 0.2 V. DC current

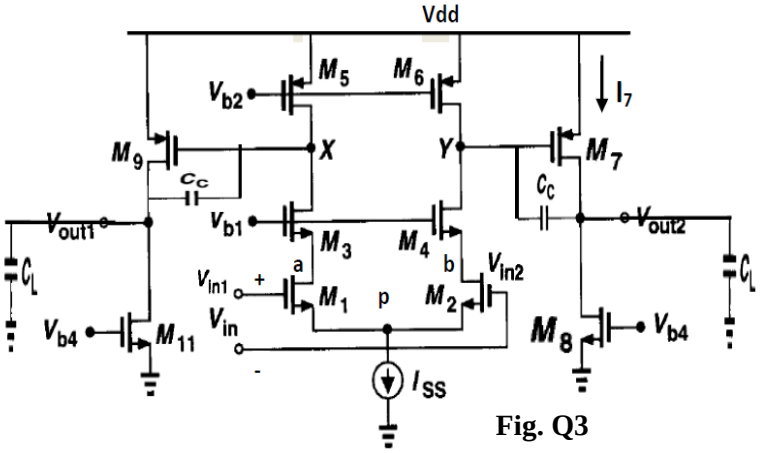

Fig. Q3

I_7 = Iss= 60uA, C_{OX}=0.04 pF/um^2, C_L= 10pF

Using approximate method

(Without Cc in the circuit--------)

(i). Calculate small signal voltage gain (A=V_{out}/ V_{in}) at low frequencies. Calculate Cgs of all transistors.

(ii). Write expressions for all pole and zero frequencies of the circuit. Express them in decreasing order of magnitude. Calculate value of each pole/ zero frequency. Take C_{gs}>C_{gd}>C_{db} with a difference of an order in their values.

(iii). Neatly Sketch and label Bode magnitude and phase (corner) plots. The plot need not be to the scale but should be logically correct. Determine phase margin and ,hence, comment upon the stability of operational amplifier

With Cc in the circuit--------

(iv). Determine the new value of dominant pole frequency to obtain a phase margin of 45 degrees. Hence compute the value of compensation capacitor 'Cc' required.

[15M]

Q4 (A) Consider the NMOS inverter given in the Fig.Q4A. Assume that the bulk terminals of all NMOS devices are connected to GND. Assume that the input IN has a 0V to 2.5V swing. V_{T0} = 0.43 V and $|\Phi_F|$ = 0.3 V.

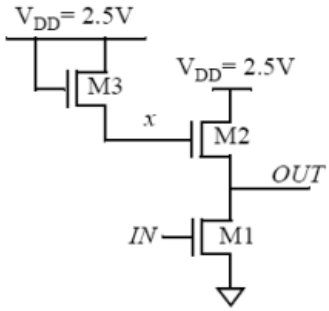

Fig. Q4A

(i). Calculate the voltage at node x. Assume γ=0.5.

(ii). What are the regions of operation of device M2? Assume γ=0 for M2.

(iii). What is the value of the output node *OUT* for the case when *IN* =0V? Assume γ=0.

[6]

Q4 (B) For the low swing buffer shown in Fig. Q4B,

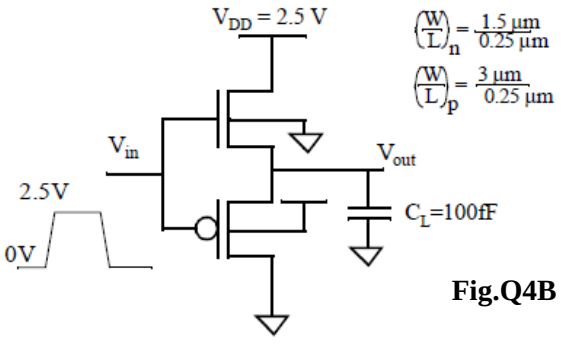

Fig.Q4B

(i). Calculate the voltage swing at the output node (V_{out}). Take V_{tn0} = 0.43V and V_{tp0} = -0.4 V , $\mu_n C_{ox}$ = 140 µA/ V^2, $\mu_p C_{ox}$ = 40 µA/ V^2

(ii). Calculate the t_{pLH} .Use average current method for calculating the current. Assume that rise and fall times of the input are 0.

(iii). Calculate the energy drawn from the power supply for a 0 V to 2.5 V transition at the input. Assume that rise and fall times of the input are 0.

[7]

Q5 (i) Implement the following function using 3 stages of NP domino logic indicating the clock signals. Start with NMOS stage. Each stage should perform some logic computation other then inversion. Inputs available are A, B, D , F, and H

$$Y = \overline{F.(\overline{\overline{A.B}} + \bar{D}) + H}$$

(ii) What are the limitations for each input transition for proper operation of each stage?

(iii) For circuit of part (i) If V_{DD}= 5 V, V_{IH}=2.9V, V_{IL}=1.9 V, $I_{leakage}$=1 pA (maximum leakage current in each stage), pre-charge and pre-discharge time of each stage is 2 ns and worst evaluation time of each stage is 10 ns. Given C_x (parasitic capacitance) = 10 fF load capacitance at each node out1, out2, and out3. Now calculate maximum and minimum frequency of operation?

(15 M)

*****All the Best *****