BIRLA INSTITUTE OF TECHNOLOGY AND SCIENCE, PILANI
EEE C443/ EEE F313/ INSTR F313: Analog and Digital VLSI Design
I- Semester 2017-2018
Comprehensive Exam (Open Book)

DATE: 11.Dec.2017 **M.M-100**
TIME: 3 hrs

General Instructions to the candidate

Please write your answers legibly and neatly.

Symbols, constants, terminology used have their usual meaning unless specified specially.

*There are a total of **FIVE** questions and all are compulsory. Each carries marks as indicated.*

*Answer the **sub-parts** of a question at one place and in the order in which they appear.*

*Preferably start each question on a **fresh page** however sub parts can be written in continuation.*

***Common data**: Use the following common data if not mentioned specifically in the question*

For 0.5µm Technology node $V_{DD} = 3.3V$, $V_{Thermal} = 25.9mV$

- *Use long channel approximation and lambda based design rules unless specially mentioned.*
- *Use square law current equation unless specifically mentioned.*
- *Neglect body effect, channel length modulation if not mentioned specifically.*
- *The body of all PMOS is tied to V_{DD} while all NMOS is tied to ground unless specially mentioned.*

Q1 Answer the following-

(I). For Fig. Q1, each flip flop has:

- Setup time of 3 ns
- Clock-to-Q maximum delay of 4ns
- Clock-to-Q minimum delay of 2ns
- Each AND/OR gate has:
  Propagation delay of 5ns
  Contamination delay of 3ns.
- NOT gate has min delay of 1ns and max 2ns, while XOR gate has min delay of 2ns and maximum delay of 8ns.

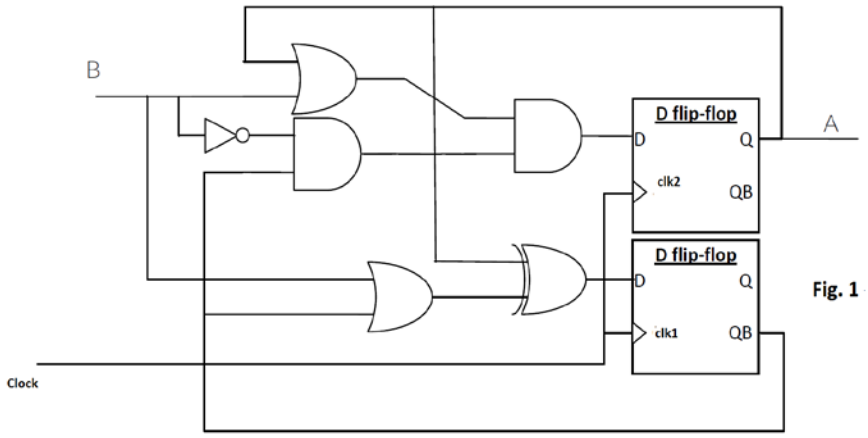

Fig. 1

a) What is the highest clock frequency that could be safely used on this circuit? Clearly show your calculations at one place.

b) In order for this circuit to work correctly, what would be the acceptable value for the hold time requirement of the D flip-flops? Clearly show your calculations at one place.

c) Now, assume a clock skew of 6ns between Clk-1 and Clk-2**,** Now, identify whether there is any timing violation. If yes, then propose the remedy and justify your calculations without changing clock frequency.

(13M)

(II). In order to drive a large capacitance (C_L = 20 pF) from a minimum size inverter gate (with input capacitance C_{IN} = 10fF), you have decided to introduce a two-staged buffer. Assume that the propagation delay of a minimum size inverter is 70 ps. Also, assume that the input capacitance of a gate is proportional to its size.

a) Determine the sizing of the two additional buffer stages that will minimize the propagation delay.

b) If you could add any number of stages to achieve the minimum delay, how many stages would you insert? What is the propagation delay in this case?

(7M)

Q2 Answer the following-

(I). A CPU design consumes 0.3mW/MHz when fabricated using a 0.13 µm process. The area of the design is 0.7 mm^2. Assume a 200 MHz clock frequency, and 1.2 V power supply. Take long channel devices.

a) If the supply voltage of the CPU design (scaled to 90 nm) is reduced to 1V, What will be area, frequency, power consumption and power density.

b) What supply voltage should be fixed to keep the power density equal to the original power density (without scaling). Also find new frequency and power consumption? Mention the type of scaling.

(II). An NMOS transistor is fabricated with the following physical dimensions and dopant concentrations: t_{ox} = 200 Å, W = 10 µm, L_m (Mask length of channel) = 1.5 µm, L_D (length of drain region) = 5µm, x_d (overlap) = 0.25 µm, x_j = 0.4 µm, $N_D = 10^{20}$ cm^3, Substrate Doping $N_A = 10^{16}$ cm^3, Channel Stop Implant Doping N_A (side wall) = $10^{19}cm^3$, Φ_o (junction built-in potential under zero bias) =0.933 V, Φsw_o (sidewall junction built-in potential under zero bias) = 1.111V

$C_{jo} = 2.98*10^{-8}$ F/cm^2, $C_{jswo} = 8.23*10^{-7}$ F/cm^2. Assume an abrupt junction.

a) Determine the capacitance at drain junction for V_{DB} = 5V

b) Calculate the overlap capacitance between gate and drain.

[20M]

Q3 Answer the following-

a) Implement the following function using 3 stage TSPC logic style such that each stage performs some logic computation (where, first stage implements A+BC). Inputs available are A, B, D, F, and H.

$$Y = [F + (A + BC).D]H$$

b) What are the limitations for each input transition for proper operation of each stage?

c) For circuit of part (a) If V_{DD}= 2.5 V, V_{IH}=1.6 V, V_{IL}=0.8 V, $I_{leakage}$=0.9 pA (maximum leakage current in each stage), pre-charge and pre-discharge time of each stage is 0.8 ns and worst evaluation time of each stage is 4 ns.

d) (Given total capacitance at each output node is 6 fF (i.e. before each tristate inverter and after each tristate inverter present in each stage). Now calculate maximum and minimum frequency of operation? Assume 50 % Duty Cycle of clock.

[20M]

Q4 Consider a CMOS inverter of (fig. 4) with following specifications where switching threshold (V_M) is 1.25 V.

V_{DD}=2.5 V, V_{T0N} = 0.4 V, V_{T0P} = -0.4 V, $\mu_n C_{OX}$=120 μA/V^2, $\mu_p C_{OX}$=40 μA/V^2, L_n=L_p=1 μm

a) Now, V_M must be reduced from 1.5 V to 1 V. Due to layout constraints, only adjustable parameter is width of n-MOS (W_n). If, W_n=2 μm when V_M =1.25 V, what is the new W_n for V_M=1 V.

b) Voltage transfer characteristics (VTC) of the above CMOS inverter (V_M =1.25 V and W_n=2 μm) is shown in Fig. 4. Calculate the gain A_v (Fig. 4) of the CMOS inverter considering λ_n=λ_p=0.235 V^{-1}

c) Calculate V_{IL} and V_{IH} from Fig. 4 using the gain (A_v) of CMOS inverter. Also, calculate the value of NM_L and NM_H.

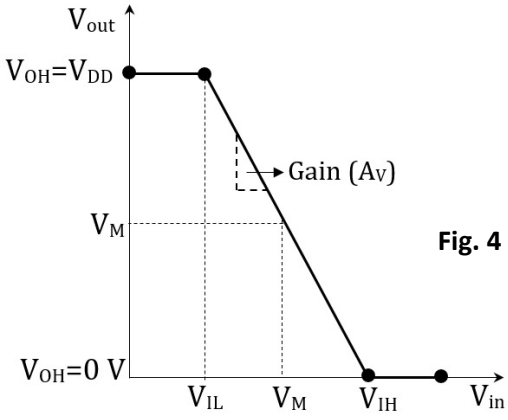

Fig. 4

[20 M]

Q5 For the OPAMP circuits shown in Fig.5 (a), and (b). r_o. . Take load capacitance at node Vout1 and Vout2= C_L. Iss is implemented with basic current mirror circuit. Given Vdd=3V, Vin (dc)=1V, Vgs of all transistors =0.9V, Vtn= lVtpl =0.7V, $\lambda_{p,n}$=0.01 V^{-1},

Do the following parts (i to v) for fig. 5(a), and fig. 5(b) separately. And fill the results in Table1. (make this table in your answer sheet)

a) Determine D.C. voltage at nodes x, m, Vb1. Hence determine ICMR.
b) Identify the amplifier configuration with following transistors--(M1, M2, M3, M4), (M5, M7), (M9, M11)
c) Intuitively, determine the expression for overall differential small signal gain 'Adm'= [(Vout1-Vout2)/ vin].
d) Intuitively, determine the expression for pole frequency at node x, node n, and node Vout1. Neglect parasitic capacitances. Identify dominant pole/ s
e) Neglecting zero/s and non-dominant poles, qualitatively find phase margin and comment on stability of OPAMP in feedback mode.
f) Intuitively, derive the expression for zero frequency due to mirror node n. In fig. 5a, what will happen to zero frequency if gate connection of M9, and M10 transistor is connected to x, and y nodes respectively.
g) Sketch and label a circuit to generate Vdd and temperature variation compensated Iss.

[20]

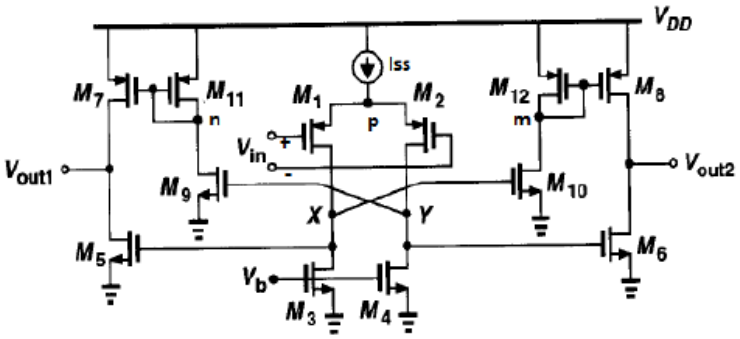

Fig. 5(a)

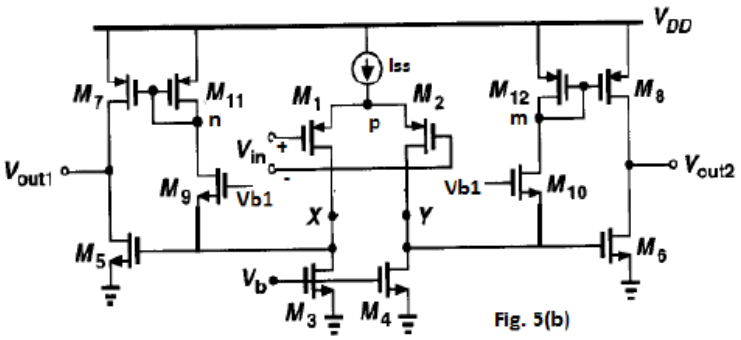

Fig. 5(b)

Table-1

	Fig. 5(a)	Fig. 5(b)
D C VOLTAGE:		
• X		
• Y		
• M		
• N		
• Vout1		
• Vout2		
ICMR		
Amplifier Configuration:		
• (M1, M2, M3, M4)		
• (M5, M7)		
• (M9, M11)		
Adm= [(Vout1-Vout2)/ vin]		
Pole frequency:		
• Node x		
• Node m		
• Node vout1		
Phase margin **Stability**		
Zero frequency due to mirror node n ($\mathbf{w_z}$)		
