Birla Institute of Technology and Science Pilani (Rajasthan)
Department of Electronics and Electrical Engineering
Analog Digital VLSI Design (EEE/INSTR F313)

Date : 13/10/2017 **MID TERM EXAM**
Time:90 min **Closed book** **Max.Marks:80**

General Instructions to the candidate

- *Please write your answers legibly and neatly in the answer booklet provided only.*
- *Symbols, constants, terminology used have their usual meaning unless specified specially.*
- *There are a total of **FOUR** questions and all are compulsory. Each carries marks as indicated.*
- *Answer the **subparts** of a question at one place and in the order in which they appear.*
- *Preferably start each question on a **fresh page** however sub parts can be written on same side.*

Common data: *Use the following common data if not mentioned specifically in the question*

Take Vdd=2.5 V, V_{T0N}=0.4V, V_{T0P} = -0.43V, R_{nmos}= 13kohm/ (W/L), R_{pmos}= 31kohm/ {W/L), Lmin=250 nm, λn=0.06 V^{-1} , λp= 0.1 V^{-1}, u_nCox= 115 uA/ V^2, u_pCox= 30 uA/ V^2

- *Use **square law current equation** unless specifically mentioned. Use lambda based design rules unless specially mentioned.*
- *Neglect body effect, channel length modulation if not mentioned specifically.*
- *The body of all PMOS is tied to V_{DD} while all NMOS is tied to ground unless specially mentioned.*

Q1 A sequential state machine was fabricated in a 10 μm technology and was able to operate at 100 MHz, consuming 10 watts using a 2 V power supply.

a) Determine the maximum frequency of operation and power consumption of the circuit if the circuit is redesigned using 5 μm technology and operating at same 2 V supply voltage?

b) Determine the maximum frequency of operation and power consumption of the circuit at 5 μm technology if operating at supply voltage of 1 V in part (a)?

c) For part (b), what supply voltage should be used to fix the power consumption at 5 watts? At what speed would the state machine operate now?

[20]

Q2 Consider a CMOS inverter with (W/L)p=1/1, (W/L)n=4/1. Assume Cwire=0.2pF, V_{DD}=5V, μ_PCox=200μA/V^2, μ_NCox=500μA/V^2, |Vtp|=Vtn=1V
For load capacitance calculation, use capacitances in Table 1 in addition to Cwire.

a) Compute the values of V_{OL}, V_{OH} voltage levels for reduced input voltage swing that varies between 0V to 3.3V

b) Now assume that Vin can swing rail-to-rail (0V to V_{DD} = 5V.) Find t_{pLH} & t_{pHL} assuming an ideal step input by averaging the appropriate currents at the beginning and end of the output transition. Use capacitances in Table 1 in addition to Cwire.

c) Find the dynamic power consumption at the output, given an input switching frequency of 100 MHz.

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Capacitor (pF)	PMOS	NMOS
C_{gs}	0.05	0.2
C_{gd}	0.05	0.2
C_{db}	0.1	0.4
C_{sb}	0.1	0.4

Table .1

Q3 Consider the inverter circuit in Fig. 1 where both load and driver are enhancement type long channel n-MOS transistors. Both the n-MOS transistors are identical except $W_{Driver} = 8W_{Load}$.

a) Calculate V_{OH}, and V_{IL} of the inverter. Also calculate V_{OL} when input (V_{in}) is V_{OH}.

b) What is the noise margin for low signal level? Consider, V_{DD}=2.5 V, V_{Tn}=0.4 V, γ=0 and λ=0.

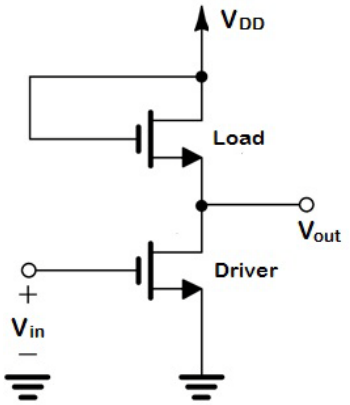

Fig .1

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Q4 A resistor of 1KΩ is to be fabricated using n-type diffusion. The n-type layer has a sheet resistance of 100 Ω per square. The width allowed for n-type layer is 1 μm. Also, 0.5 μm extension of metal and n-type layer is required over the contact window. [Note: size of contact pad = 1 μm x 1 μm]

a) Determine the length of n-type diffusion layer required.

b) Sketch and label the layout of the n-type layer. Include the area for placing contact cuts in your layout.

c) Now, sketch and label the layout of contact cuts to be placed on the n-type layer.

d) Also, sketch & label the layout of metal layer to be placed over the n-type layer.

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