BIRLA INSTITUTE OF TECHNOLOGY & SCIENCE, PILANI - K. K. BIRLA GOA CAMPUS

FIRST SEMESTER, 2019-2020

MID-SEMESTER EXAMINATION, Analog & Digital VLSI Design (EEE F313/INSTR F313)

Closed Book **Maximum Marks: 60** **Duration : 90 Minutes** **Date 04.10.2019**

Q1. For the differential amplifier shown below in **figures 1 and 2**, assume that the (W/L) value of each transistor ($100\mu m/1\mu m$). **Do calculations for figure 1 and figure 2 separately.** Use V_{DD}=1.5 V.

(a) Find the maximum input common mode voltage, $v_{IC}(max)$ and the minimum input common mode voltage, $v_{IC}(min)$. Keep all transistors in saturation for this problem.

(b) What is the input common mode voltage range, ICMR?

(c) Find the small signal voltage gain, v_o/v_{in}, if $v_{in} = v_1 - v_2$.

(d) If a 10 pF capacitor is connected to the output to ground, what is the -3dB frequency for $V_o(j\omega)/V_{in}(j\omega)$ in Hertz? (Neglect any device capacitance.)

(e) Out of figure 1 and 2, which is better amplifier? Why?

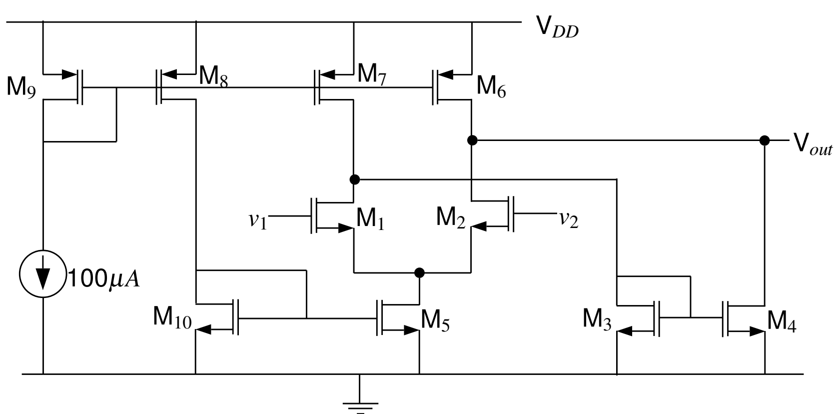

Figure 1: Q1.1

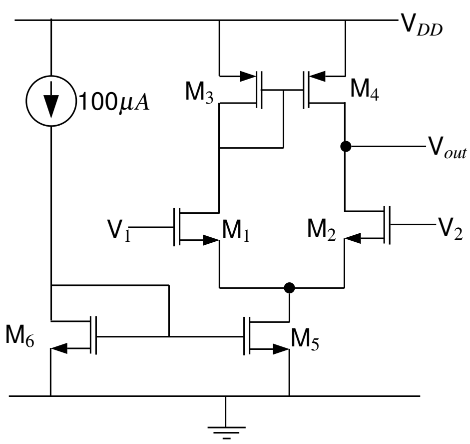

Figure 2: Q1.2

Given : **NMOS:** $\mu_n C_{ox} = 110 \ \ \mu A/V^2$, $\lambda_n = 0.04V^{-1}$ for L=1 μm, V_{tn}=0.7 V
PMOS: $\mu_p C_{ox} = 50 \ \ \mu A/V^2$, $\lambda_p = 0.05V^{-1}$ for L=1 μm, V_{tp}=-0.7 V

(Marks:4+2+4+4+2)

Q2. Find the slew rate, SR, of the differential amplifier shown in **Figure 3** where the output is differential. Repeat this analysis if the two current sources, $0.5I_{SS}$, are replaced by resistors of R_L. **(Marks:2+2)**

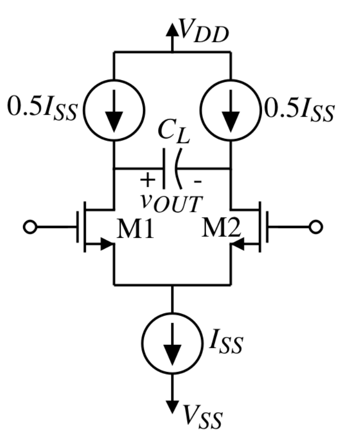

Figure 3: Q2

Q3. Design a two-stage op amp based on the topology shown in **figure 4**. Assume a power budget of 6 mW, a required output swing of 2.5 V, and L = 0.5 μm for all devices. Use V_{DD}=3 V.

(a) Allocating a current of 1 mA to the output stage and roughly equal overdrive voltages to M_5 and M_6, determine $(W/L)_5$ and $(W/L)_6$. Note that the gate-source capacitance of M_5 is in the signal path, whereas that of M_6 is not. Thus, M_6 can be quite a lot larger than M_5.

(b) Calculate the small-signal gain of the output stage.

(c) With the remaining 1 mA flowing through M_7, determine the aspect ratio of M_3 (and M_4) such that V_{GS3}=V_{GS5}. This is to guarantee that if V_{in} = 0 and hence V_X=V_Y, then M_5 carries the expected current.

(d) Calculate the aspect ratios of M_1 and M_2 such that the overall voltage gain of the op amp is equal to 500.

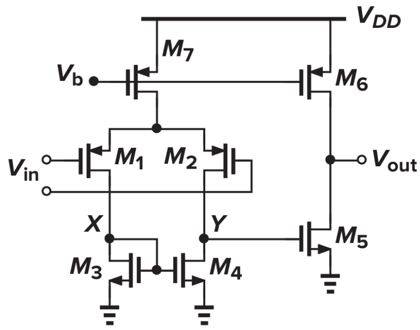

Figure 4: Q3

Given : **NMOS:** $\mu_n C_{ox} = 134 \ \ \mu A/V^2$, $\lambda_n = 0.1V^{-1}$ for L=0.5 μm, V_{tn}=0.7 V
PMOS: $\mu_p C_{ox} = 38 \ \ \mu A/V^2$, $\lambda_p = 0.2V^{-1}$ for L=0.5 μm, V_{tp}=-0.8 V **(Marks:4+4+4+4)**

Q4. An nMOS transistor is fabricated with the following physical parameters: $W = 10\ \mu m$, $L_M = 1.5\ \mu m$ (Mask length), $L_D = 0.25\ \mu m$. Calculate the oxide related capacitance, c_{gd}, c_{gs} and c_{gb} for all three regions of operations. Assume oxide thickness of $t_{ox} = 200\ \AA$. **(Marks:9)**

Given : $\varepsilon_{ox} = 3.9 \times 8.85 \times 10^{-14} F/cm$, $\varepsilon_{Si} = 11.7 \times 8.85 \times 10^{-14} F/cm$, $q = 1.6 \times 10^{-19} C$, $kT/q = 0.026\ V$, $n_i = 1.45 \times 10^{10}\ cm^{-3}$

Q5. For symmetric CMOS inverter if NM_L=1.2 V, V_{IH}=1.8 V, what will be the threshold voltages of NMOS and PMOS used in CMOS inverter? **(Marks:3)**

Q6. The circuit of **figure 5** is designed with $(W/L)_1 = 50/0.5$, $I_{D1} = I_{D2} = 5\mu A$, and $R_D = 1k\Omega$.

(a) Determine $(W/L)_2$ such that the contribution of M_2 to the input-referred thermal noise current (not current squared) is one-fifth of that due to R_D.

(b) Now calculate the minimum value of V_b to place M_2 at the edge of the triode region. What is the maximum allowable output voltage swing? **(Marks:6+6)**

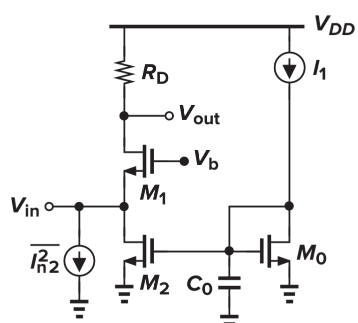

Figure 5: Q5

Given : **NMOS:** $\mu_n C_{ox} = 134 \ \ \mu A/V^2$, $\lambda_n = 0.1V^{-1}$ for L=0.5 μm, V_{tn}=0.7 V
PMOS: $\mu_p C_{ox} = 38 \ \ \mu A/V^2$, $\lambda_p = 0.2V^{-1}$ for L=0.5 μm, V_{tp}=-0.8 V