1. (*12 marks*) Answer the following questions
   a. Assume a ring oscillator using 5 CMOS inverters, provides a signal with 45% duty cycle and a period of 2ns. What is the rise and fall time of the inverter in this technology?
   b. Calculate the noise margins at node a and node b in the circuit in figure 1(b).
   c. In the circuit shown in figure 1 (c), calculate the voltages at nodes A, B, C, D and E. It is given that $V_{DD} = 1\,V$, $V_{Tn} = 0.25\,V$ and $V_{Tp} = -0.35\,V$, $L = 100nm$. The caps are 0.1pF.
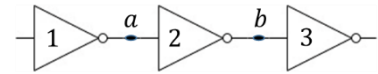
INV	V_{OH} (V)	V_{OL} (V)	V_{IH} (V)	V_{IL} (V)
1	1.8	0.1	1.3	0.5
2	2.0	0.2	1.6	0.3
3	2.0	0.0	1.4	0.6

Figure 1 (b)

2. (*10 marks*) Consider a pseudo-NMOS inverter with the following parameters, $V_{Tn} = -V_{Tp} = 0.4V$, $V_{DD} = 3.3V$, $k'_n = 100\,\mu A/V^2$ and $k'_p = 40\,\mu A/V^2$, $(W/L)_n = 4(W/L)_p = 12$. Assume that a load of 100fF is connected to this circuit. Neglecting the effect of self-loading of the transistor, calculate the L-H (50%) delay for this gate. You may need the following formula

Figure 1 (c)

$$\frac{1}{(a+x)(b-x)} = \frac{1}{(a+b)}\left\{\frac{1}{a+x} + \frac{1}{b-x}\right\}$$
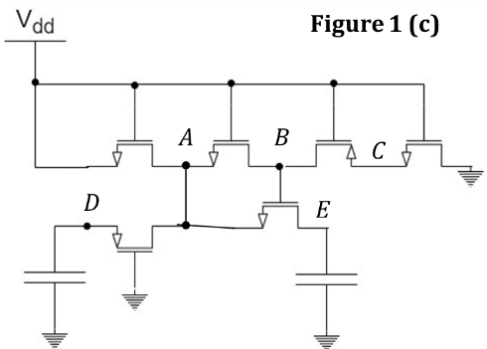

3. (*10 marks*) In order to implement OR4 logic to drive a 10fF on-chip capacitance, we end up with two options, (A) NOR4(1X)+INV(5X) or (B) NOR2(2X)+NAND2(?X). Assume the reference is a 2/1 sized inverter, and the gate and diffusion capacitance per unit width is $C = 1.25\,fF/\mu m$. Calculate the size ratio of NAND2 in option (B) to make the two options achieve the same delay. Assume the minimum CMOS transistor width ($W_p + W_n$) is 80nm. The convention NOR2(BX) means that the transistors in the NOR2 gate are sized B times larger than the smallest NOR2 gate in the technology.
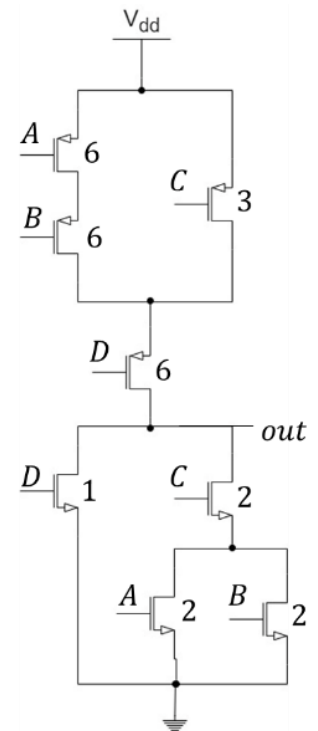
4. (*10 marks*) Consider the complex logic gate in figure 4. The widths of the transistors are given. Assume that the minimum width NMOS transistor has an on-resistance of R, a gate cap of C and a S/D cap of C. The smallest inverter is of size P/N=2/1. There is no sharing of diffusions. When calculating delays assume that the internal nodes are charged or discharged as appropriate
   a. Find the contamination delay for the rising and falling transition and identify the input transition for the same.
   b. Find the Elmore delay for the following transitions (ABCD)
      i. (1111)→(1100)
      ii. (0000)→(1010)

Figure 4

5. (*10 marks*) Find the sizes of the transistor in the circuit in figure 5, for least delay from input to out. G2 is an AOI gate. Draw the circuit and indicate the sizes clearly along with the input that is in the critical path. The input inverter is minimum sized with P/N=2/1.
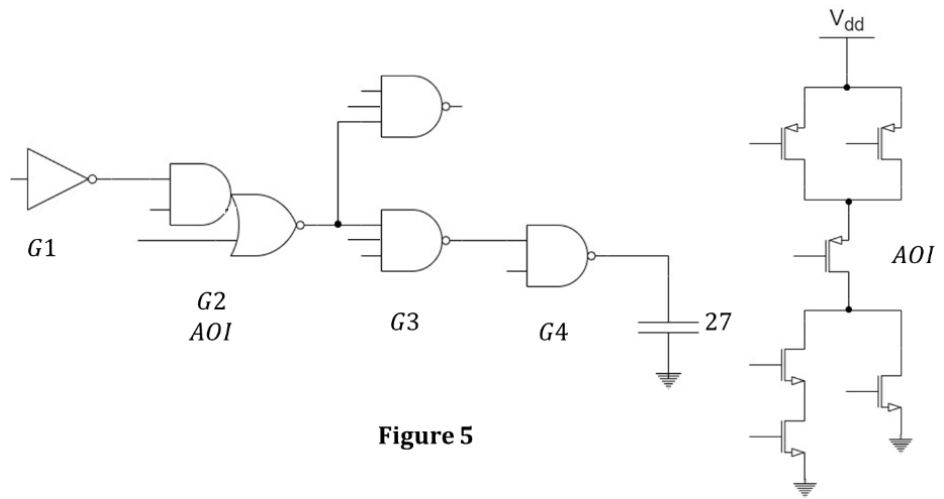

Figure 5

6. (*9 marks*) The sequential circuit in figure 6, has 2 flip-flops and 2 combinatorial blocks CB1 and CB2. The design is made using a library that includes inverters with 25ps rise and fall delay. The parameters for the flops are: $t_{pcq} = 100\ ps$, $t_{ccq} = 20\ ps$, $t_{setup} = 50\ ps$, and $t_{hold} = 100\ ps$. The parameters for the CLBs are as follows CB1: $t_{pd} = 250\ ps$, $t_{cd} = 100\ ps$ and CB2: $t_{pd} = 350\ ps$, $t_{cd} = 50\ ps$.

Figure 6

   a. Will the circuit work correctly? Explain and; if not, suggest a fix to the flip-flop parameters that will not affect the maximum frequency at which the circuit can be operated.
   b. If the circuit can be operated correctly, what is the maximum CLK frequency at which it will work correctly?
   c. Suggest modification in the CLK circuitry to increase the frequency found in (b). Explain your solution.
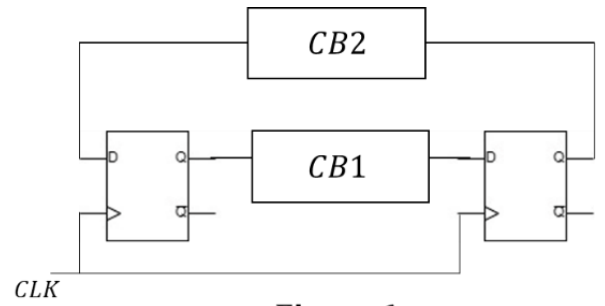
7. (*9 marks*) Answer the following questions
   a. An amplifier with forward gain A_0 has two coincident poles at ω_p. Calculate the maximum value of A_0 for a 60° phase margin with closed loop gain of (i) unity and (ii) 4.
   b. An amplifier has a forward gain of $A_0 = 1000$ and two poles at ω_{p1} and ω_{p2}. For $\omega_{p1} = 1\ MHz$, calculate the unity-gain feedback loop if (i) $\omega_{p2} = 2\omega_{p1}$ and (ii) $\omega_{p2} = 4\omega_{p1}$.

8. (*10 marks*) Design a differential input single ended output amplifier; **with input applied to a PMOS pair**; for output voltage swing of 0.8 V. The total bias current is $100\mu A$. The size of all transistors should be equal. Keep minimum length as $1\mu m$. $\mu_n C_{ox} = 300\ \mu A/V^2$, $\mu_p C_{ox} = 65\ \mu A/V^2$, $V_{Tn} = 0.36\ V$, $V_{Tp} = -0.5\ V$. Use $\lambda_n = 0.11\ V^{-1}$ and $\lambda_p = 0.09\ V^{-1}$, $V_{DD} = 1.8\ V$
   a. Draw the circuit diagram
   b. Find the overdrive voltages of all transistors
   c. Find the W/L of all transistors
   d. Find $V_{in,cm,max}$ and $V_{in,cm,min}$.
   e. Calculate the gain of the amplifier

******** All the best ********