

Q1. Design differential input, single ended output telescopic operational amplifier (single stage) with following specifications: (all calculations for 2 significant digits).

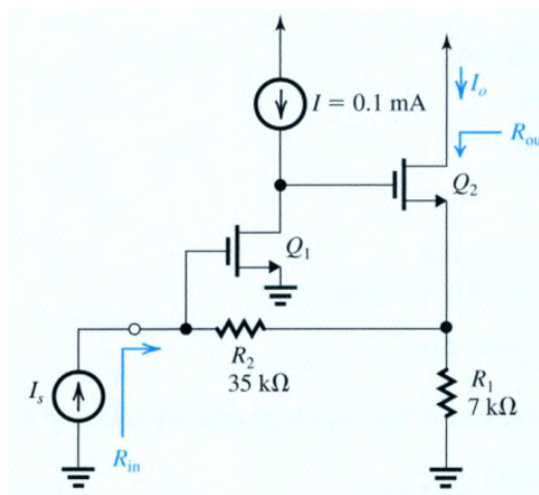
(Given: $V_{thn} = -V_{thp} = 0.4V$, $\mu_n C_{OX} = 2\mu_p C_{OX} = 200\mu A/V^2$, $\lambda_n = 0.1V^{-1}$, $\lambda_p = 0.2V^{-1}$ for $L=0.5\ \mu m$, $V_{DD} = 3\ V$)

- For load capacitor of 20 pF, slew rate is 5 V/ μs .
- Output voltage swing = 1.6 V.
- All transistors are almost of the same size.
- Tail current source is single transistor NMOS current mirror.

Find $\frac{W}{L}$ values of all transistors (neglect λ for size calculation). What is input common mode voltage range? What is gain of the amplifier? What is the output voltage swing if output is shorted with inverting input of amplifier?

Q2. The feedback current amplifier in figure utilizes two identical NMOS transistors (Q_1 and Q_2) sized so that at $I_{D1} = 0.1\ mA$ they operate at $V_{ov} = 0.2\ V$. Both Q_1 and Q_2 have $V_t = 0.5\ V$ and $V_A = 10\ V$. The DC current source (labeled as I) is realized by PMOS as current source with $V_t = -0.5\ V$ and $V_A = 20\ V$.

- (a) If I_s has zero DC component, what is the DC current flowing through Q_2 ? What is the DC voltage at the input (at the gate of Q_1)?
- (b) Find the ideal value of $A_f = I_o/I_s$, and the value of β .
- (c) Find g_m and r_o for each of Q_1 , and Q_2 .
- (d) Find the A circuit and the value of R_{in} , A, and R_{out} without feedback with loading effect.
- (e) Find loop gain and gain with feedback.
- (f) Find R_{in} and R_{out} with feedback.



Q3. In a feedback amplifier, the transfer function of feed-forward amplifier is given by

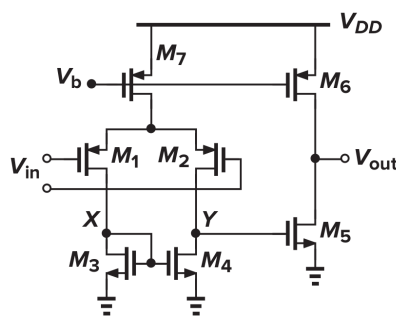
$$A(s) = \frac{10^5}{\left(1 + \frac{s}{2\pi \times 10^5}\right) \left(1 + \frac{s}{2\pi \times 10^7}\right) \left(1 + \frac{s}{2\pi \times 10^9}\right)}$$

The feedback factor β is independent of frequency.

- (a) For what value of β , the phase margin of loop gain will be 0° ? What is gain crossover frequency?
- (b) For what value of β , the phase margin of loop gain will be 60° ? What is the gain margin for this value of β ?
- (c) At gain crossover frequency, the closed loop gain exhibits overshoot of 11.5 times the closed loop DC gain. What is the phase margin in this case? Assume $|A\beta| \gg 1$.

Q4. Design a two-stage op amp based on the topology shown in figure. Assume a power budget of 6 mW, a required output swing of 2.5 V, and $L = 0.5 \mu m$ for all devices. Use $V_{DD}=3 V$. (Neglect λ while calculating sizes of transistors).

- (a) Allocating a current of 1 mA to the output stage and roughly equal overdrive voltages to M_5 and M_6 , determine $(W/L)_5$ and $(W/L)_6$. Note that the gate-source capacitance of M_5 is in the signal path, whereas that of M_6 is not. Thus, M_6 can be quite a lot larger than M_5 .
- (b) Calculate the small-signal gain of the output stage.
- (c) With the remaining 1 mA flowing through M_7 , determine the aspect ratio of M_3 (and M_4) such that $V_{GS3}=V_{GS5}$. This is to guarantee that if $V_{in} = 0$ and hence $V_X=V_Y$, then M_5 carries the expected current.
- (d) Calculate the aspect ratios of M_1 and M_2 such that the overall voltage gain of the op amp is equal to 500.



Given : **NMOS:** $\mu_n C_{ox} = 134 \mu A/V^2$, $\lambda_n = 0.1V^{-1}$ for $L=0.5 \mu m$, $V_{in}=0.7 V$

PMOS: $\mu_p C_{ox} = 38 \mu A/V^2$, $\lambda_p = 0.2V^{-1}$ for $L=0.5 \mu m$, $V_{tp}=-0.8 V$

Q5. The following is known about a CMOS inverter circuit. $V_{Tn}=-V_{Tp}=0.4 V$, $V_{DD}= 3.3 V$. Assume $\left(\frac{W}{L}\right)_n =4$ and $\left(\frac{W}{L}\right)_p =12$. Assume $k'_n = 100\mu A/V^2$ and $k'_p = 40\mu A/V^2$. Assume square law model for the MOSFETs. You may neglect channel length modulation. Determine

- (a) The input switching threshold voltage of the inverter.
- (b) The input voltage when the output is 3.1V
- (c) The input voltage when the output is 0.2V