Birla Institute of Technology and Science Pilani (Rajasthan)
Department of Electrical and Electronics Engineering
EEE F313/ INSTR F313, Analog and Digital VLSI Design
First Semester

[Time: 90 min]

Date: 13 Oct 2023 **Mid-semester Test (Closed Book) FN1** **Max. Marks: 75**

General Instructions to the candidate

- *Please write your answers legibly and neatly in the answer booklet provided only.*
- *Symbols, constants, terminology used have their usual meaning unless specified specially.*
- *There are a total of **Four** questions, and all are compulsory. Each carries marks as indicated.*

Unless specifically mentioned—

Common data: *Use the following common data (250nm technology) if not mentioned specifically in the question*

Take Vdd=2.5 V, Lmin= Wmin =250 nm, R_{nmos}= 13kohm/ unit (W/L), R_{pmos}= 31kohm/ unit (W/L),

V_{T0N}=0.4V, V_{T0P} = -0.4V, λn=0.1 V^{-1} , λp= 0.1 V^{-1}, u_nCox= 120 uA/ V^2, u_pCox= 40 uA/ V^2

- *Use **square law current equation** unless specifically mentioned. Use lambda based design rules unless specially mentioned.*
- *Neglect body effect, channel length modulation if not mentioned specifically.*
- *The body of all PMOS is tied to V_{DD} while all NMOS is tied to ground unless specially mentioned.*
- *Label your sketches properly.*

Answer all the subparts of a question together in sequence.

Q1. Consider the design of a CMOS circuit in 90 nm technology node to implement the Boolean function appended below:

$$F = \overline{(A+B)(C+D)}$$

a) Sketch and label its transistor-level schematic.

b) Hence, find all the possible Euler's path.

c) Hence, sketch and label its stick diagram for Eulers path ABCD.

d) Estimate the cell area from stick diagram.

e) Hence , sketch and label the cross-sectional diagram across p-diffusion region.

[20 marks]

Q2. The layout of a PMOS is given in Fig.1. Use the parameters given in this question.

$V_{TOP} = -1V$, $K'p = 20\ \mu A/V^2$, $C_{ox} = 69$ nF$/cm^2$, $C_{jsw} = 2.2$ pF/cm , $C_{jo} = 7$ nF$/cm^2$, $K_{eq,p} = 0.5$ $(for\ all\ kind\ of\ junctions)$, $L_D = 1\ \mu m$, W $= 10\ \mu m$, P $= 14\ \mu m$, Q $= 6\ \mu m$, R= $8\ \mu m$,

$x_j = 32\ nm$, $t_{ox} = 1.5\ nm$, Lmask=5um

a) Calculate value of gate (C_{gb}), drain (C_{gd}) and source (C_{gs}) oxide capacitances when MOS is in linear and saturation region of operations , respectively.

b) Calculate total junction capacitance of the device (source + drain region) under the state of thermal equilibrium. (Assume **No conduction** in the channel and No external bias is applied at any of the terminals of the PMOS)

c) Now calculate the total junction capacitance (source + drain region) when device is operating in linear region with a swing from 0-V_{DD}.

[15 marks]

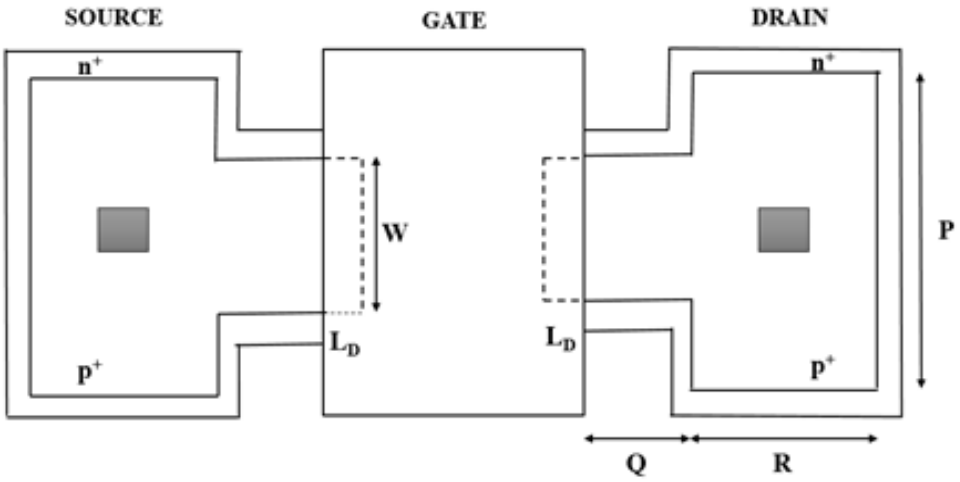

Fig. 1

Q3. Consider the CMOS inverter schematic shown in the Fig. 2.

Ignore channel length modulation, body bias effect, and parasitic capacitances

All transistors have the same ON resistance 'R' and $\mathbf{NM_H = NM_L}$. The $\mathbf{V_{out}}$ value corresponding to $\mathbf{V_{IH}}$ is **0.5V**

a) Determine the values of $\mathbf{V_M, V_{IL}, V_{IH}, N_{ML}, N_{MH}}$.

b) Now, assume all NMOS transistors become fast by **20%,** and all PMOS transistors become slow by **20%.** Determine the new values of $\mathbf{V_M, V_{IL}, V_{IH}}$.

Here, assume the same $\mathbf{V_{out}}$ values **for** $\mathbf{V_{IL}}$ and $\mathbf{V_{IH}}$ as in part (a).

[20 marks]

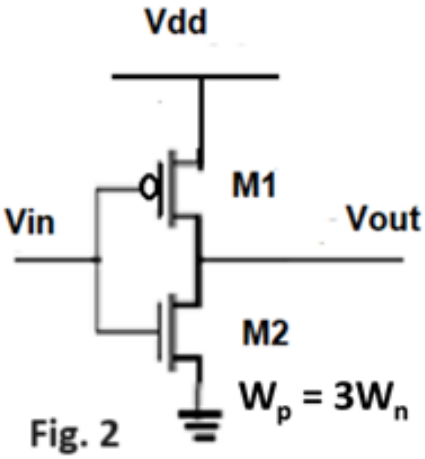

Fig. 2

Q4. Consider circuit shown in Fig. 3, Given that node labeled as 'X', has total capacitance value C_x=20 fF. The transistor sizes are given as ----:

$(W/L)_{M1} = (W/L)_{M2} = (W/L)_{M3} = 3$

$(W/L)_{M4} = 3$ [P-Tree is a complement of N-Tree

where each PMOS device has same aspect ratio of $(W/L)_{M4}$]

a) Derive and calculate value fall time "τ_{fall}" at node 'X' (here take **V_{DD} to 10 % of V_{DD}**). (Assume the default device parameters mentioned at start and ideal step inputs. [*Use differential equation based formula/method for all the delay calculation]*

b) Hence, calculate maximum short circuit power consumption of first stage of Fig. 3. Assume , for input waveform, 'τ_{fall}' = 'τ_{rise}' and has same value as calculated in part (a)] . Given input frequency is 1 MHz.

[20 marks]

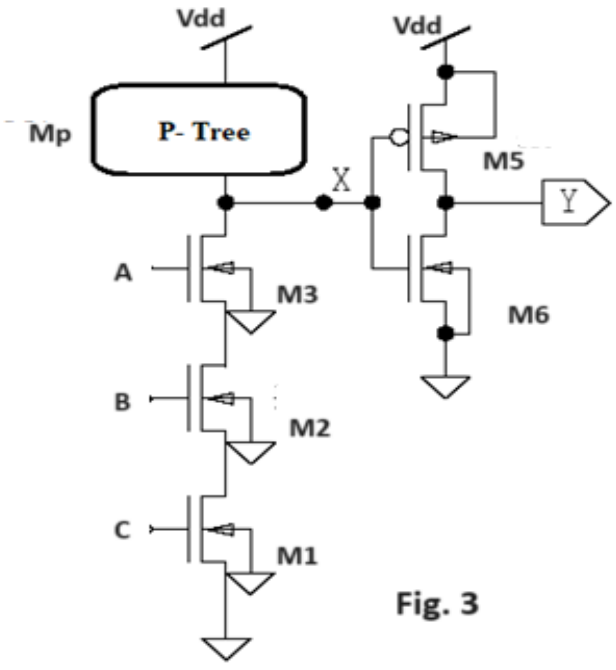

Fig. 3

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