EEE F313/ INSTR F313: Analog and Digital VLSI Design
I- Semester 2023-2024
Comprehensive Exam (Open Book)

DATE: 15 Dec. 2023, FN (9 -12) am **M.M—105 marks TIME: 3 hrs**

Total (3+3 questions)
***Common data**: Use the following common data **if not mentioned specifically** in the question*
For 0.25µm Technology node -- Lmin=250 nm,

Take Vdd=2.5 V, V_{T0N}=0.4V, V_{T0P} = -0.4V, R_{nmos}= 13kohm/ (W/L), R_{pmos}= 31kohm/ {W/L),
C_{OX}=6 fF/ µm^2, λn=0.1 V^{-1} , λp= 0.1 V^{-1}, u_nCox= 90 uA/ V^2, u_pCox= 30 uA/ V^2

g(inv)=1, p(inv)=1 for standard cmos inverter

- *Use long channel approximation and lambda-based design rules unless specially mentioned.*
- *Use square law current equation unless specifically mentioned. Neglect channel length modulation in current calculation, if not mentioned specifically. The body of all PMOS is tied to V_{DD} while all NMOS is tied to ground unless specially mentioned.*

Answer the sub-parts of a question at one place and in the order in which they appear.

SECTION - A (60 marks total)

Q1. The layout shown in Fig.1 is a pull up network of a digital circuit designed in 180 nm technology node. Dimensions of different parameters are labeled in the layout itself.
For this layout,
-- area junction capacitance is **$C_j = 3 \times 10^{-4}$ pF/µm^2,**
---side wall junction capacitance is **$C_{jsw} = 2 \times 10^{-4}$ pF/µm**
--- (W/L) = 20.

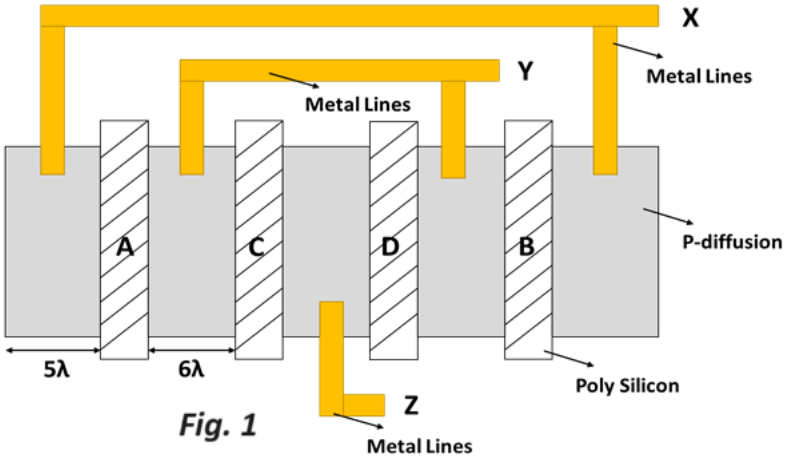

Fig. 1

Answer the following questions :

a) Calculate the width of each transistor.
b) Write down the Boolean function represented by the given layout considering, X = V_{DD}, Y = Intermediate node, Z = Output node.
c) Calculate the total source to bulk junction capacitance for the given layout. Here ignore the overlap capacitance.
d) Calculate the total drain to bulk junction capacitance for the given layout. Here ignore the overlap capacitance.
e) Sketch & Label the layout of pull down network in the same format as in Fig.1. Clearly mention the source and drain terminals of each transistor in your drawing.

[20 marks]

Q2. A CMOS inverter , with minimum sized transistors . Assume **K_n =0.2mA/V^2, K_p = 0.1mA/V^2 and Vt_n=|Vt_p|=0.6V, V_{DD} = 3.3V.**

a) Calculate the inverter gate switching threshold voltage V_M ?

b) What is the resistance for each transistors using our general expression for MOSFET resistance in saturation?

c) Determine the rise and fall times of this circuit if the parasitic capacitance at the output is 9fF (use RC delay model)?

d) Also, calculate the propagation delays for this circuit if a load capacitances of 25fF is added at the output (use RC delay model)?

e) Now, a ring oscillator (of 11-stages) is created using given CMOS inverter. Determine the frequency of operation of ring oscillator in megahertz (MHz). Hence, compute power delay product for one CMOS inverter stage for given (load + parasitic) capacitance driven by it. Assume dynamic power consumption is dominant.

[20 marks]

Q3. Answer the following— Ignore the channel length modulation effect in the calculation.

Take **$\mu_n C_{ox}$= 100 µA/V^2, $\mu_p C_{ox}$= 50 µA/V^2, V_{T0N}=0.4V, V_{T0P} = -0.5 V.**

a) Consider the inverter circuit shown in **Fig. 2 (a)**. Identify the topology of the inverter circuit. Hence, determine $\left(\frac{W}{L}\right)_{MN}$ of NMOS Transistor (M_N) such that the low output voltage, **V_{OL}≤ 100 mV.**

Take, $\left(\frac{W}{L}\right)_{Mp} = \frac{3\mu m}{0.18\ \mu m}$, for the PMOS Transistor.

(b). Now, consider the CMOS Inverter circuit shown in ***Fig. 2 (b)***

Given $\left(\frac{W}{L}\right)_{MN} = \frac{5\mu m}{0.18\ \mu m}$, **and** $\left(\frac{W}{L}\right)_{Mp} = \frac{11\mu m}{0.18\ \mu m}$

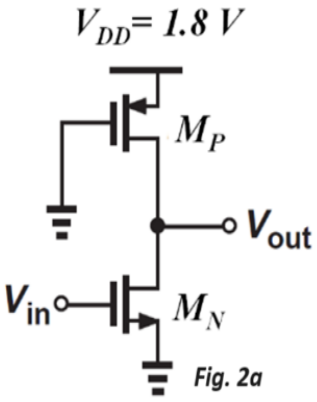

Fig. 2a

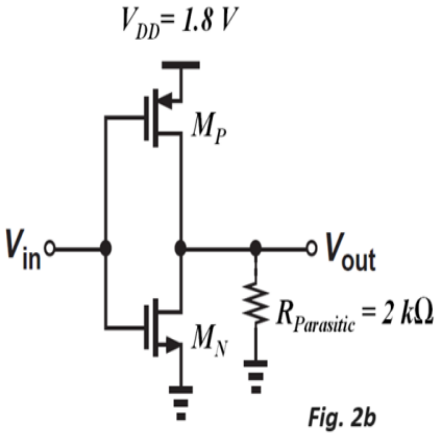

Fig. 2b

Without $R_{parasitic}$ in Fig. 2b circuit, determine the value/s of----

i. **V_{OL}** (Low output voltage), and **V_{OH}** (High output voltage)

ii. **V_{IL}** (Low input voltage) for Vout =Vdd. Also find **V_{IH}** (High input voltage) for Vout=0V

iii. **$(NM)_L$** (Noise Margin Low), and **$(NM)_H$** (Noise Margin High).

iv. Hence, sketch and label the Voltage Transfer Characteristics **(VTC**) for **Fig. 2b** circuit.

With parasitic resistance, $R_{parasitic}$, present in Fig. 2(b)--

v. Qualitatively explain the effect of ***$R_{parasitic}$*** on the values of **V_{OL}** (Low output voltage), and **V_{OH}** (High output voltage).

[20 marks]

----------Section A ends----------

Write the section name clearly on top of each sheet.

Answer the sub-parts of a question at one place and in the order in which they appear.

SECTION - B (Total 45 marks)

Neglect body effect

Q4. Consider the circuit shown in **Fig. 3**. Assume ***μn= 2 μp***. All transistors have length as **Lmin= 0.25 um**

a) Write down the Boolean expression for ***G*** node.

b) Can we add a CMOS inverter between node ***F*** and ***Gate 2***? Briefly justify your answer.

c) Assuming the switching threshold of the inverter/s **(INV1, INV2) is 1.5 V.**

Assume capacitance [**Cx= 5fF (at node *X*) , Cp= 30fF** (at node ***P***)] for ***Gate 1***,

and **[C_D =24fF, C_Q=15fF, C_N=10fF]** for ***Gate2***

Now, calculate the output voltage (worst-case values) at node G during the evaluation state

(**Φ=LOGIC '1'**) under the following inputs:

i. $A_0 = 1, B_0 = 0, A_1 = 1, B_1 = 0.$
ii. $A_0 = 1, B_0 = 1, A_1 = 1, B_1 = 0.$

d) What is wrong with the calculated voltage at **node G** in the later part of **part (c)?** explain.

What is the remedy for this?

e) Determine the minimum path delay $\bar{D}$ **(**from input A_0 to G) during the evaluation phase using the logical effort method. Take **H= 50** for calculation. Assume the reference CMOS inverter is designed with ***μn= 2 μp*** has ginv=1, pinv=1.

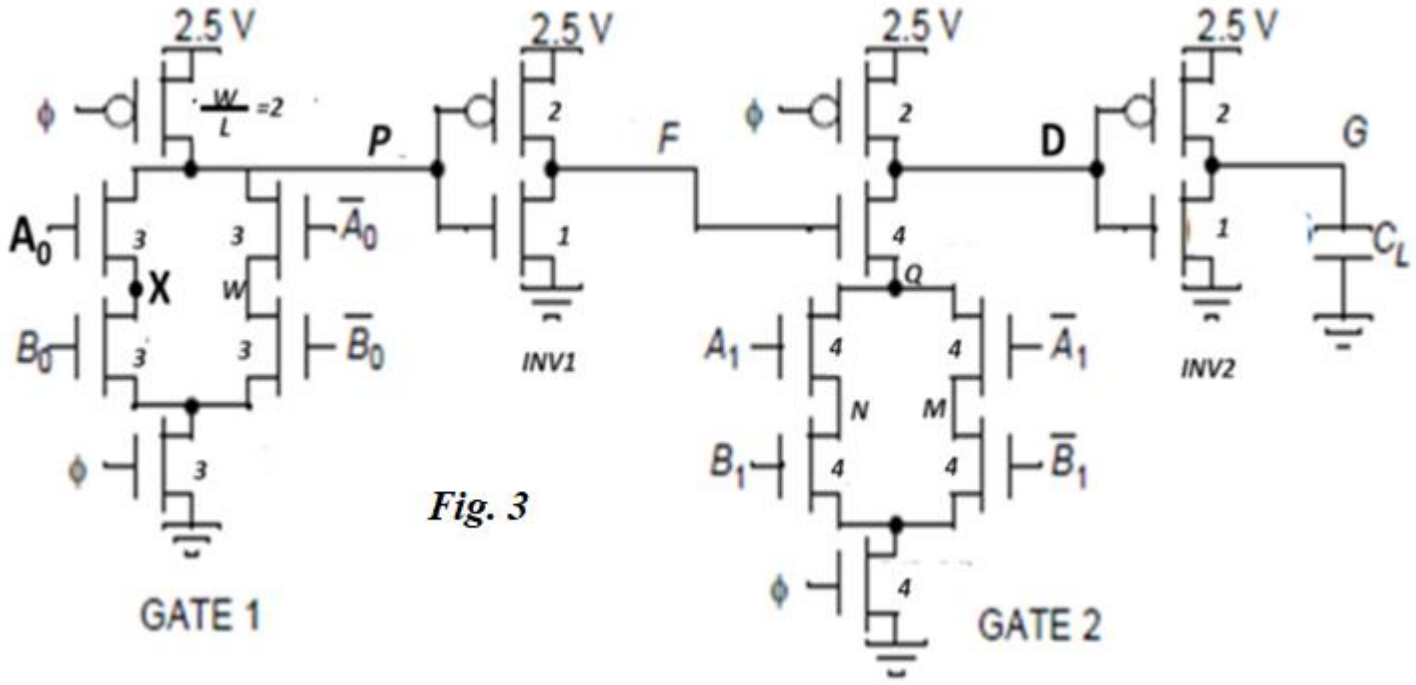

Fig. 3

[20 marks]

Q5. For the operational amplifier (OPAMP) circuit shown in **Fig. 4** the maximum input voltage (V_{id}) for which output enters in slew mode is **0.282 V.**

Given:[M4, M5, M6, and M7] are matched, [M2, and M3] are matched)

---**Stage-1** transistors M1 , M2 and M3 have the same overdrive voltage (Vov).

---The total capcitance at $\mathbf{V_{out2}}$ i.e. $\mathbf{CL_2}$ **is 0.5 pF** and slew rate is **200 V/μSec** .

---**Stage 2** has a bias current of **50 μA** and an overdrive voltage of **0.2 V.**

(use common data given on the first page for calculations)

Now, Calculate the following for the OPAMP:---

a) If **ICMR is 1.7 V** then find the overdrive voltage (**Vov.)** of the transistors M4, and M6.

b) **Find V_{out2} (DC), $V_{out2(max)}$, $V_{out2(min)}$.**

c) Find Differential low-frequency small signal gain intuitively **(V_{out3}/V_{id})**

d) Estimate C_{L3} such that the pole at the Vout3 node appears at **12.5 Mrad/sec**

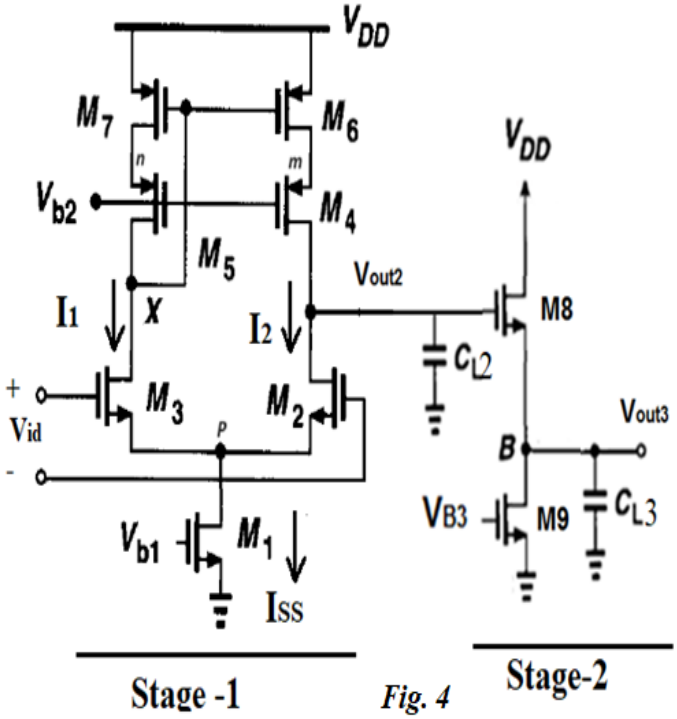

Fig. 4

[15 marks]

Q6. Consider the circuit shown in **Fig. 5**. Iss is a basic current mirror circuit.
Assume, all transistors have the same Vov=**0.2V, λ=0.01V^{-1}**

- Load capacitance is $\mathbf{C_L}$ **= 10pF** at output node/s Vout.
- Load capacitance is $\mathbf{C_{x,y}}$ at output node/s Vx,y.
  Given, $\mathbf{C_1=C_{X,Y}= 0.5\ C_L}$.
- Given [M1, M2, M5, M6], [M7, M8] , [M3, M4], [M11, M12, M9, M10] are matched transistor pair/s.

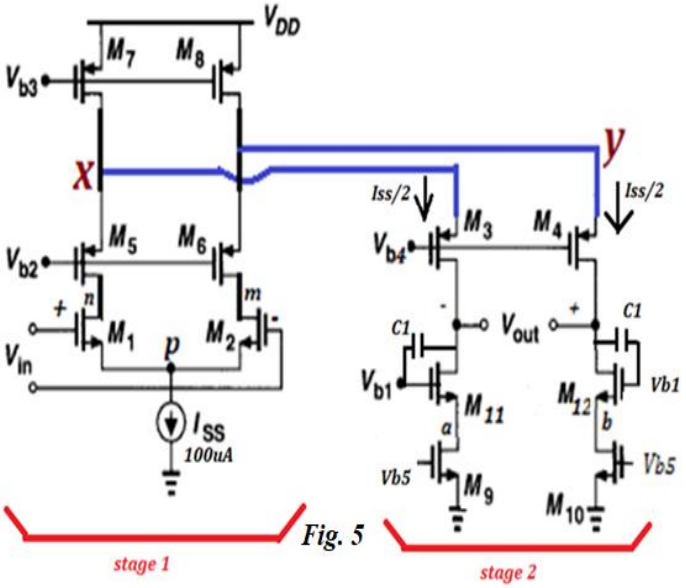

Fig. 5

a) Identify the operational amplifier (OPAMP) topology.

b) Determine the value for low-frequency (dc) small-**signal differential voltage gain** $\left[\frac{v_{out}}{v_{in}}\right]$ intuitively in dB.

c) Also, determine values of pole frequencies at node,/s **Vx** , and **Vout** intuitively.

d) Hence, estimate the unity gain bandwidth (**UGB**) of the circuit.

e) Now, sketch and label the Bode Magnitude (corner) plot (not to the scale, but qualitatively correct)

[10 marks]

----------Section B ends----------