Birla Institute of Technology and Science, Pilani

II semester 2017-2018

EEE F341 /INSTR F341 Analog Electronics

Comprehensive Exam (Closed Book)

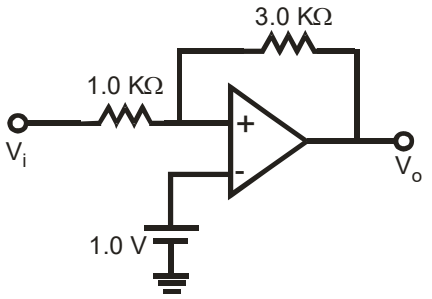
Date: 07/05/2018 **Duration: 100 minutes** **M.M.: 60**

There are *Four* questions. Answer all sub-parts of a question at one place.

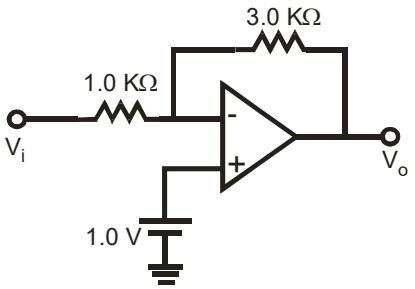
Note: Assume Op-Amp to be ideal and V_{sat}=±12 V until or unless specifically mentioned.

Q.1 (a) Design a multirange voltmeter using V-I converter to have 2 MΩ input impedance and can measure 0-100 mV, 0-10V and 0-100 V. Use PMMC to show the output assume full scale deflection as 100 μA and meter resistance as 10 KΩ. Extend the design to measure same range AC voltages (RMS) also using only half wave rectifier at suitable place. **[9M]**

Q.1 (b) Draw transfer characteristic for the circuits (Vsat=±12 V). **[6M]**

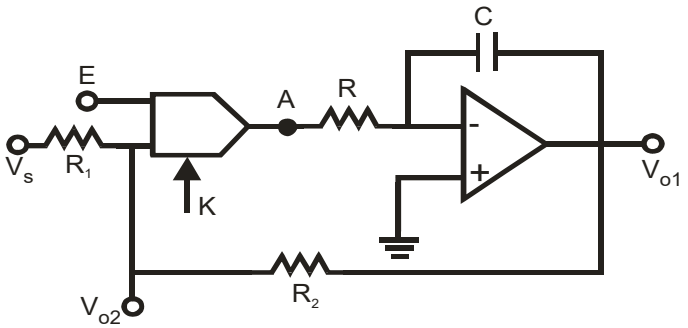


Circuit (a)

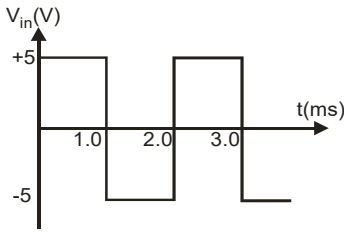


Circuit (b)

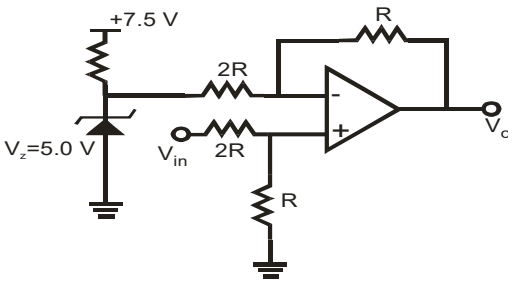
Q.2 (a) Find the transfer function at V_{o1} and V_{o2} for the given circuit and also sketch and label bode magnitude plot for V_{o2} assuming $R_1 = R_2$, R = 10 KΩ, C = 0.1μF and E = 1 V. (K = 10) **[7M]**



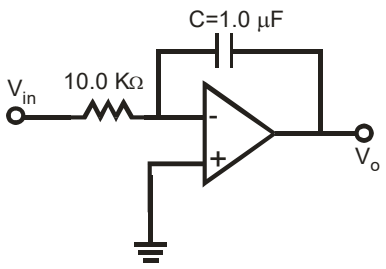
Q.2 (b) Sketch and label V_o for the given circuit if given input is applied. **[8M]**



Input



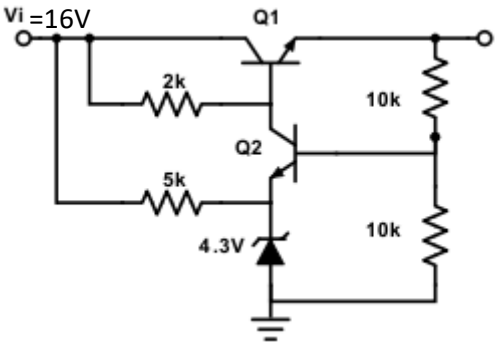
Circuit (a)



Circuit (b)

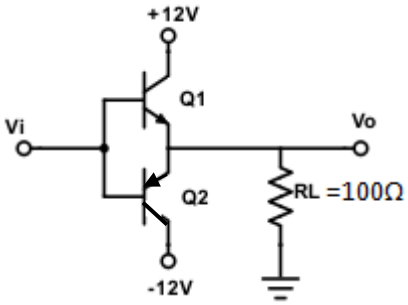
P.T.O.

Q.3 (a) For the given circuit, find S_V, R_O, V_O. Implement current limit for $i_{L(max)}$ = 100mA. Also find power dissipation through Q1 and zener diode when maximum current is being drawn.
($\beta_{Q1} = 50, \beta_{Q2} = 100, r_z = 10\Omega, V_{BE} = 0.7V$, ignore r_x, r_Π) **[8M]**

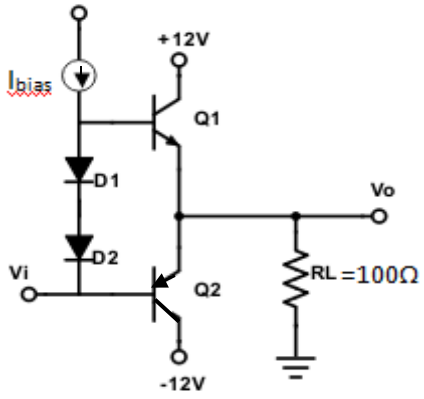


Q.3 (b) Design an astable free running multivibrator using opamp to generate 10kHz frequency having 40% duty cycle (T_H/T). Use β = 0.1, C = 10nF and V_{sat} = ±10V. **[7M]**

Q.4 (a) i) Sketch and label transfer characteristics for circuits (a) and (b) shown below.
($V_{CE} \approx 0, V_{BE} = 0.5V, \beta = 40$ for all transistors)



Circuit (a)



Circuit (b)

ii) In circuit (b), assume junction areas of Q1 and Q2 are double of the biasing diodes and biasing diodes require minimum of 1mA current. Find Quiescent current and quiescent power dissipation of the output transistor. **[3+3=6M]**

Q.4 (b) A tuned intermediate frequency (IF) amplifier for FM is to be designed using two synchronous tuned stages with central frequency of 10MHz. Find-

i) The required bandwidth of single stage to produce overall bandwidth of 200KHz.
ii) Use a 3μH inductance and find R, C for each stage.
iii) Suggest a suitable circuit to avoid output-input coupling of tank circuits. **[2+3+1=6M]**

Q.4 (c) An 8-bit ADC uses 6.4 V as reference voltage. Find-

i) Full scale range,
ii) Analog voltage corresponding to 00010111,
iii) Same analog voltage calculated in (ii) is to be converted using dual slope integrator having R=40kΩ and C=0.1μF. If the integrator is connected to analog voltage for 10ms, then find the peak voltage across integrator output. **[2+2+2=6M]**

**********End**********