Birla Institute of Technology and Science, Pilani

EEE F341/INSTR F341 Analog Electronics

Second Semester 2021-2022, Comprehensive Exam

Part A (CLOSED BOOK)

Time: 85 min **Max. Marks: 50** **Date: 06-05-2022**

Name: **ID:**

Note: Assume all op-amps have V_{Sat}= ± 10 V, if not mentioned in the question.

Question no. 1 to 10: Each question carries one mark. √ the correct answer.

(1) The other name of voltage follower is
(a) Differential amplifier (b) Inverting amplifier
(c) Non-inverting amplifier (d) Unity gain amplifier

(2) A regulated power supply has
(a) Error amplifier (b) Series pass transistor
(c) Feedback network (d) All of the above

(3) A general second order filter has roll-off rate
(a) -20 dB/decade (b) -10 dB/decade
(c) -40 dB/decade (d) -30 dB/decade

(4) Select correct statement of PLL
(a) Capture range smaller than lock range (b) Lock range smaller than capture range
(c) Capture range is equal to lock range (d) None of the above

(5) In PLL, name of phase detector is
(a) Adder (b) Subtractor
(c) Multiplier (d) Divider

(6) The gain of an op-amp decreases at high frequency due to
(a) Capacitance (b) Resistance
(c) Gain (d) None of the above

(7) VCO is designed so that at zero voltage it is oscillating at some initial frequency called
(a) Cut-off frequency (b) Free-cycle frequency
(c) Corner frequency (d) Free-running frequency

(8) Find the maximum frequency for a sine output voltage of 10 V peak with op-amp whose slew rate is 1 V/μs
(a) 16 kHz (b) 15 kHz
(c) 14 kHz (d) 12 kHz

(9) Gain of differentiator using op-amp is
(a) $\omega R_f C_1$ (b) $\omega / R_f C_1$
(c) $-j\omega R_f C_1$ (d) $1/\omega R_f C_1$

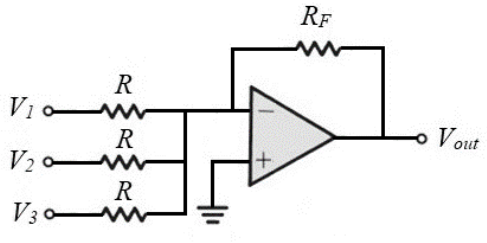
(10) A second order filter has two poles at s= -0.5±j0.866 and transmission zero at 2 rad/s. What is the correct transfer function for unity gain at dc.

(a) $\frac{S^2+4}{S^2+S+1}$ (b) $\frac{1}{4}\frac{S^2+4}{S^2+S+1}$

(c) $\frac{S}{S^2+S+1}$ (d) $\frac{S+2}{S^2+S+1}$

Question no. 11 to 25: Write correct answer(s) in the blanks.

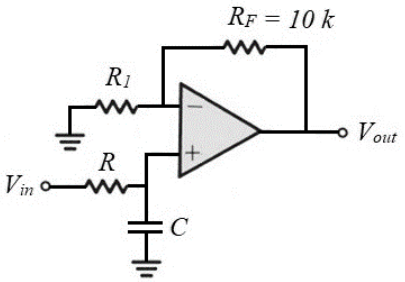
(11) In the given circuit consider the inputs like V_1 = +2 V, V_2 = +3 V, V_3 = +4 V, R_F = R = 1 kΩ and supply voltage ±15 V. Determine output voltage.



V_{out} = _____V [2]

(12) For the given filter circuit cut-off frequency is 2 kHz, pass band gain 2 and C=0.01 µF.

Find,



R = _____ kΩ [2]

R_1 = _____ kΩ [1]

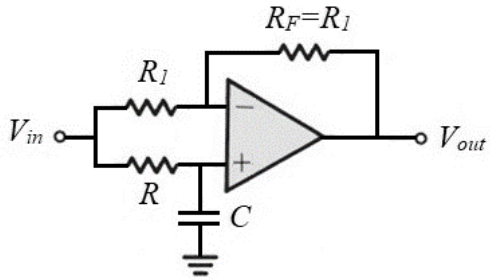
(13) Determine the voltage gain (A_f), input resistance (R_{if}) and output resistance (R_{of}) with feedback for voltage-series feedback amplifier having A= -100 (V/V), R_i = 10 kΩ, and R_O=20 kΩ for feedback factor β = -0.5.

A_f = _____ (V/V) [1]

R_{if} = _____ kΩ [1]

R_{of} = _____Ω [1]

(14) Determine the phase angle (θ) and time delay (t_d) for the circuit given for a frequency of 2 kHz, assuming R_1=20 kΩ, R= 39 kΩ, R_F=R_1 and C=1 nF.



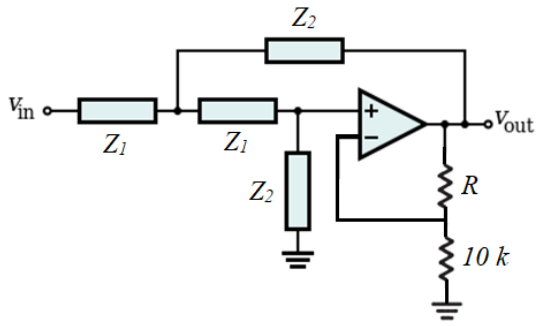
θ = _____ (degree) [2]

t_d = _____ µs [1]

(15) A first order low pass Butterworth active filter has a cut-off frequency of 10 kHz and unity gain at low frequency. Find the voltage transfer function magnitude in dB at 12 kHz for the filter. (Consider ε=1)

$|H(j\omega)|$= _____ dB [2]

(16) Design the Sallen-Key VCVS second order High Pass Butterworth filter to have 3 dB cutoff frequency of 20 kHz. Use capacitance of 1.59 nF only. Find,

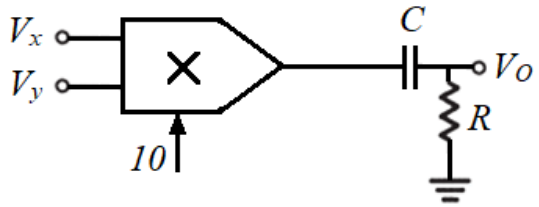


Z_1 = _____ [1]

Z_2 = _____ [1]

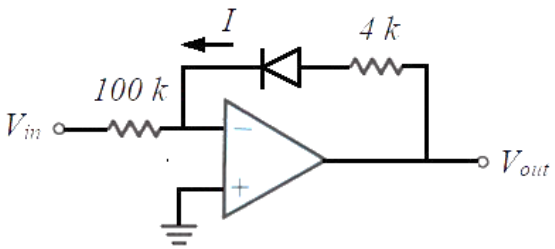
R = _____ [2]

(17) For the circuit given below find the expression for V_O assuming large value of capacitor.
Given,
$V_x = 4\,Sin(1000\pi t)$ V
$V_y = 4Sin(1000\pi t + 30^\circ)$ V



V_O = _____V [2]

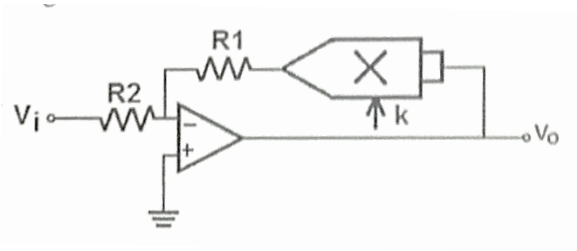
(18) Calculate I and V_{out} of the given circuit where, V_{in}= -1 V, reverse saturation current (I_S) = 1 µA and thermal voltage (V_T) = 26 mV. (Consider, η=1 for Si diode)



Current (I): _____ µA [1]

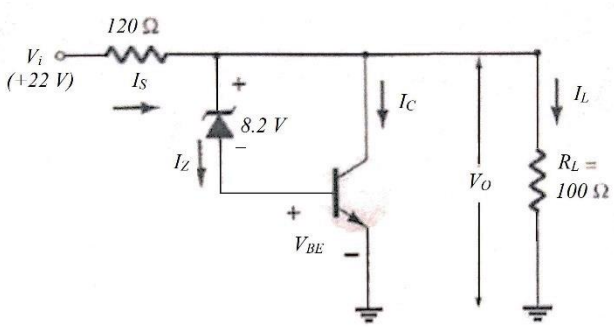
V_{out}: _____ V [2]

(19) Find V_O expression for the given circuit.



V_O = _____ [2]

(20) For the given voltage regulator circuit consider base-emitter voltage as 0.7 V. Find,



V_O = _____ V [2]

I_S = _____ A [1]

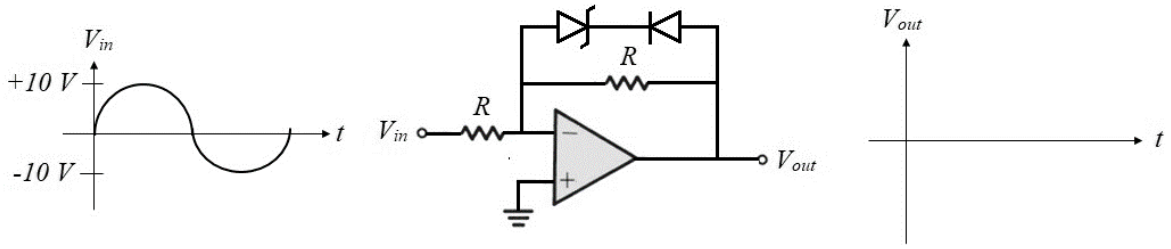
I_C = _____ mA [1]

(21) For an isolation amplifier, C_{ISO} = 2.2 pF, IMRR = 180 dB, V_{ISO}=1000 V and input signal frequency 20 MHz. Find

Impedance across isolation barrier: _____ kΩ [1]

Error voltage drawn across isolation barrier: _____ µV [1]

(22) Sketch and label V_{out} for the given circuit. Consider Zener drop 3.3 V and forward diode drop 0.7 V. For op-amp $\pm V_{sat} = \pm 12$ V. [2]

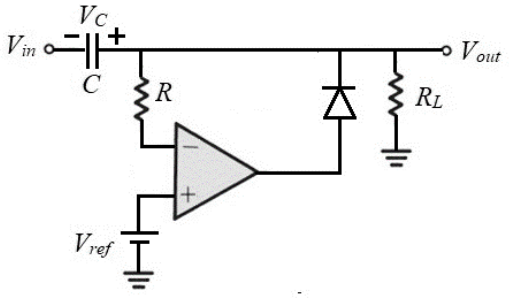


(23) For the given clamping circuit, assume V_{ref} = 1.5 V and input voltage varies from -2.5 V to 5 V Find

V_C: _____ V [1]

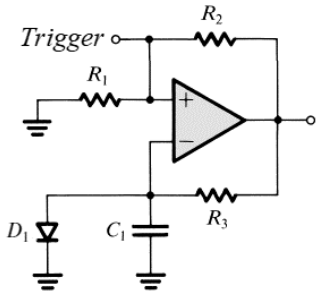
Peak value of V_{out}:_____V [1]

Maximum differential input voltage of op-amp: _____ V [1]



(24) Write the expression of the pulse width (T) for the given monostable multivibrator when V_{sat}>> forward diode drop (V_D) and R_1=R_2.

T = _____ [2]

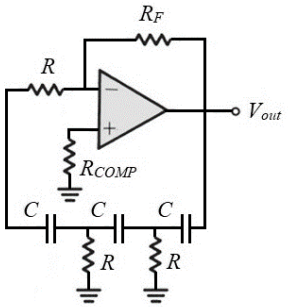


(25) For the given RC phase shift oscillator f_0=300 Hz. (Consider C = 0.1 µF)

Find,

Input resistance = _____ kΩ [2]

R_F = _____ kΩ [1]



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Second Semester 2021-2022, Comprehensive Exam

Part B (OPEN BOOK)

Time: 95 min **Max. Marks: 55** **Date: 06-05-2022**

Note: Assume all op-amps have V_{Sat}= ± 10 V, if not mentioned in the question.

Q1. For the given precision circuit shown in Fig 1, now, draw the transfer characteristics i.e V_{o1} vs V_i and V_{o2} vs V_i. Consider forward diode drop of 0.7V for D_1, D_2, and D_3. **[6M]**

Q2. Design the oscillator circuit shown in Fig.2 to sustain oscillation at 10KHz frequency with ± 6V output. Consider, forward diode drop as 0.7V. Find R_P,R_s R_2, R_4, R_5. **[8M]**

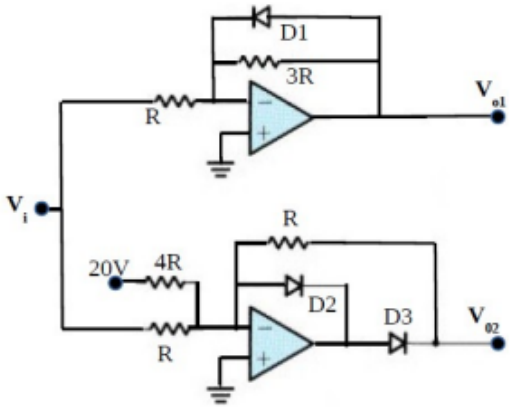

Fig. 1

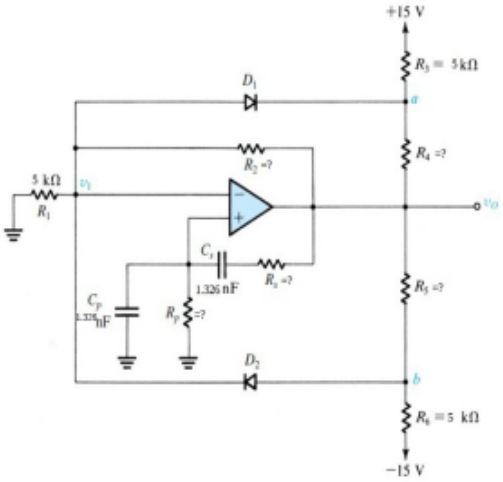

Fig. 2

Q3. For the voltage regulator circuits as shown in Fig. 3(a,b). Consider V_{BE} = 0.7V. **[12M]**

a). Find out the value of V_o, V_{CE}, I_L and I_Z for circuit shown in fig3a.

b). Find out the value of V_o, I_1 , I_L and P_{dmax} by BJT for circuit shown in fig3b.

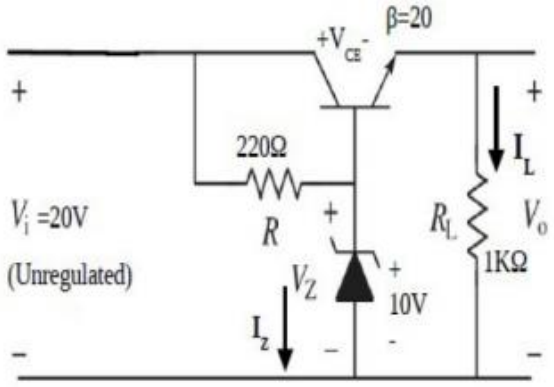

Fig. 3(a)

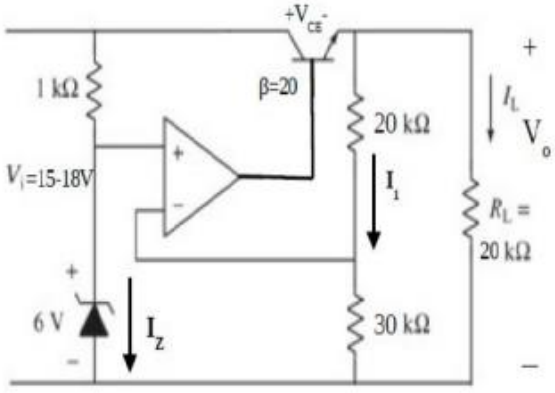

Fig. 3(b)

P.T.O

Q4. For the wave generator circuit shown in Fig. 4, find the expression of T_H, T_L and frequency (f) in form of RC. If, C = 0.1μF and R = 22.62kΩ, then draw and label V_o and V_c. (± Vsat = ±15V and $R_2 = 9R_1$).

[12M]

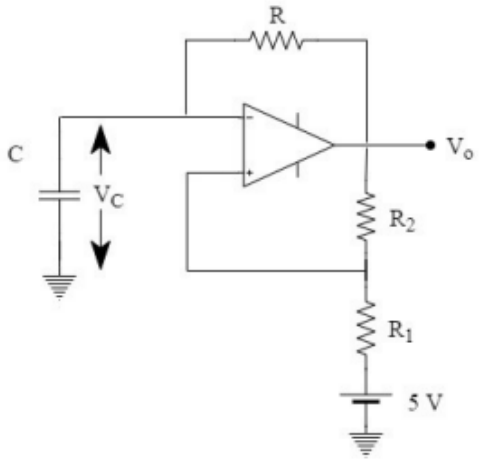

Fig. 4

Q5. For the circuit shown in Fig. 5, comment on the type of waveform to be produced at V_{01} and V_{o2}. Determine the period, frequency and peak value of the signal at V_{o1} and V_{o2}. Also, sketch and label the V_{o1} and V_{o2} waveforms. Consider $R_1 = 100k\Omega$, $R_2 = 10k\Omega$, $R_3 = 20k\Omega$, $C_1 = 0.01\mu F$ and $\pm V_{sat} = \pm 14V$.

[8M]

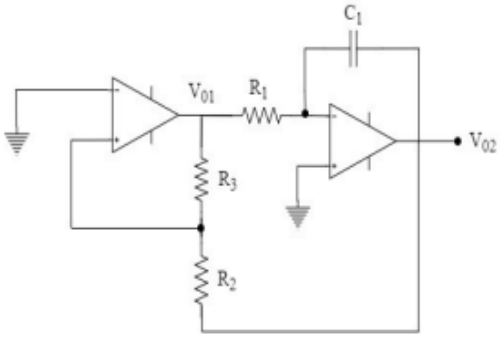

Fig. 5

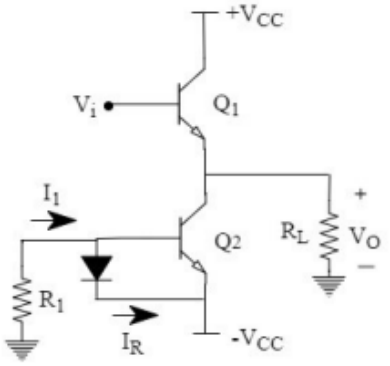

Fig.6

Q6. Design the emitter follower circuit shown in Fig. 6. Assume $V_{cc} = 12V$, $V_{BE} = 0.7V$, $V_{CEsat} = 0.5V$, $I_R = 5mA$ and $R_L = 650\Omega$.

a) Determine the critical value of load resistance to avoid distortion.

b) Calculate peak to peak output voltage swing if $R_L = 650\Omega$.

c) Also, calculate peak-to-peak output voltage swing and power efficiency (η) if $R_L = 2.5K\Omega$.

[9M]

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