BIRLA INSTITUTE OF TECHNOLOGY & SCIENCE, PILANI, RAJASTHAN

Second Semester 2021-2022
Mid Semester Test (Closed Book)

Course no: EEE F477	Max. Marks :60
Course Title: Modeling of Field Effect Nano Devices	Weightage : 30%
Date : 10-03-2022	Duration : 90 minutes

ID No : -- Name : ------------------------------------

Note: Please fill the blanks with appropriate answers OR strike off the wrong words as per the question. (This part has to be returned) 15x2=30 M ,
[Relative permittivity of Si and SiO2 as 11.8 and 3.9. ni= 1.5x10^10/cm^3, Eg= 1.12 eV, kT =0.026 eV all at room temp.]

1. (i) In a MOS transistor to reduce delay, the current should be less/more and under constant voltage scaling with K as 1.41, the device having delay of 1 ns shows a delay as --- ------.

   (ii) In one dimensional quantum well device, if the well length is halved , the E1 state energy would be -------E1 and the wave vector of the electron would be -------.

   (iii) A silicon substrate doped with 1.5x10^15 / cm^3 phosphorous impurity at room temperature having MOS capacitor with 10 nm SiO2 will show a flat band voltage as ------- with n+ metal and no oxide charge. This flat band voltage would be -------for a Qox as 10^-8 C/cm^2.

   (iv) A metal with workfunction of 4.6 eV and p-substarte doped with 1.5x10^16/cm^3 shows a V_T as 0.9 V, the VT would be --------if the doping is increased by one order of magnitude. In case if tox is increased the VT would be more/less.

   (v) In a scaled bulk MOS device the depth of drain region close to channel is same/lower/larger as compared to regions away from that end. To avoid metal contact spikes in drain region the junction depth should be more/less.

   (vi) The total capacitance of a MOS capacitor in subthreshold region at higher frequency increases/decreases/remains same with the applied metal voltage and in case of MOSFET devices at subthreshold , the capacitance increases/decreases/remains same.

   (vii) In a double gate Si/SiO2 depleted SOIMOSFET with Si thickness as 8nm , the critical length would be more than ----- nm to avoid short channel effect and this critical length is more/less if the higher dielectric is used (tox as 2 nm)

   (viii) Usually I-V characteristics of SOI DGMOSFET shows a kink effect in case of FDDGMOSFET/PDDGMOSFET and this may lead to increase/decrease in VT.

   (ix) In a thin SOI DGMOSFET case of volume inversion the effective conductance would be equal./ more/less than the sum of the individual channel conduncases and this may be due to ------------.

(x) In a FDDGMOSFET device if both the top and the bottom chnanels are in inversion, the field in the middle would be minimum/maximum/zero and the field below forward oxide will be more/less/zero if the back gate goes in accumulation.

xi. In MOS devices , the length scaling increases /decrease the threshold voltages and this becomes more/less sensitive if junction depth of S/D is increased.

xii. In a MOS device, the width scaling increases/decreases the threshold voltages and this influence can be mitigated by using --------technique for isolation.

xiii. In a MOS transistor tox reduction puts more/less gate leakage current and if the thickness of tox is to increased by 5 times , then to maintain same leakage current the dielctric constant of the oxide would be ------times.

xiv. In a bulk n-MOSFET , the punchthrough voltage changes by ------times if the length is increased by 2 times. The punchthrough volatage increases/decreases with the increase of doping.

xv. In a short channel MOS device , the carrier injection near source end is modelled as vth, this requires higher/lower channel doping near source end and needs more /less vertical electric field at that point.

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Q.2 to 6 each of 6 marks. (This set has 6 marks as bonus) ---36 M

2. Explain different process steps to make a CMOS structure on SOI based substarate and also a conventional CMOS over p-substarte mentioning any four improvements observed in SOI case. (6)

3. Sketch and label C-V characteristics across a MOS structure at low and high frequency operations. Explain the physical reasons for the extreme values of C at critical points and also sketch the case of deep depletion with proper explainantion. (6)

4. Sketch and label energy band diagram and also electric field distribution across a n+ poly Si/SiO2/p-Si (doped with 1.5x10^16/cm3). Assume voltage across SiO2 is 0.3 V. Comment on the nature of Si region just below SiO2 at Vg as 0.0 V, - 0.5 V and +0.5 V respectively. (6)

5. Sketch and label DGSOI n-MOSFET having n+ poly as gate and SiO2 as both oxides. The capacitances/area of forward and back oxides are 3.45x10^-6 F/cm^2 and 3.45x10^-7 F/cm^2 respectively and channel doping is 10 ^17 /cm^3. Assume the Si region just gets depleted when both the gates are at inversion.

   (a) Comment on the operation of the device if Si doping is increase by 4 times also comment ofn forward channel behavior if back gate voltage is changed.
   (b) Comment on the role of back gate voltage variation if back gate is changing in negative polarity.
   (c) Sketch and label potential variations from top gate to bottom gate under both channels are in inversion.
   (d) Compute VT if both channels are inverted (assume oxides are charge free).
   (e) Compute subthreshold slope(S) at room temperature under full depleted case. (12)

6. Discuss the role of DIBL in short channel and its solutions to mitigate mentioning suitable process techniques at the channel and source/drain level. (6)