BIRLA INSTITUTE OF TECHNOLOGY & SCIENCE, PILANI, RAJASTHAN

Second Semester 2022-2023
Mid Semester Test (Closed Book)

Course no: EEE F477	Max. Marks :60
Course Title: Modeling of Field Effect Nano Devices	Weightage : 30%
Date : 14-03-2023	Duration : 90 minutes

ID No : --- Name : -------------------------------------

Note: Please fill the blanks with appropriate answers OR strike off the wrong words as per the question.
(This part has to be returned) 15x2=30 M ,
[Relative permittivity of Si and SiO2 as 11.8 and 3.9. ni= 1.5x10^10/cm^3, Eg= 1.12 eV, kT =0.026 eV all at room temp, $\epsilon_0 = 8.85\times10^{-14}$ F/cm]

1. (i) In a MOS transistor to reduce delay, the current should be less/more and under constant voltage scaling with K as 1.41, the device having delay of 1 ns shows a delay as --- ------.

   (ii) In a MOS device subthreshold conduction slope S (mV/decade I) would be --------in case of Cd is Cox/3 and this would be ------if the oxide thickness is halved.

   (iii) Current drive in a fingered FINFET for a given pitch P would be smaller/greater than –- times W (assuming $w=t_si/2$). This can further be increased when pitch is increased/decreased.

   (iv) A metal with workfunction of 4.7 eV and p-substarte doped with 1.5x10^15/cm^3 shows a V_T as 0.9 V, the V_T would be --------if the doping is increased by one order of magnitude. In case if tox is increased the V_T would be more/less.

   (v) In a scaled bulk MOS device the depth of drain region close to channel is same/lower/larger as compared to regions away from that end. To avoid metal contact spikes in drain region the junction depth should be more/less.

   (vi) : For a lattice mismatch factor of 0.02 , the critical thickness required to avoid starin on the top layer would be ---times of the lattice parameter of the substarte. The mobility in the Si/Ge starined film would be enhanced /reduced.

   (vii) Usually in MOS transistor isolation in VLSI along channel length, we use LOCOS/Trench and along channel width we use LOCOS/Trench.

   (viii) Usually I-V characteristics of SOI DGMOSFET shows a kink effect in case of FDDGMOSFET/PDDGMOSFET and this may lead to increase/decrease in V_T.

   (ix) In a thin SOI DGMOSFET case of volume inversion the effective conductance would be equal./ more/less than the sum of the individual channel conductance and this may be due to ------------.

(x) In a FDDGMOSFET device if both the top and the bottom chnanels are in inversion, the field in the middle would be minimum/maximum/zero and the field below forward oxide will be more/less/zero if the back gate goes in accumulation.

xi. In MOS devices , the length scaling increases /decrease the threshold voltages and this becomes more/less sensitive if junction depth of S/D is increased.

xii. In a MOS scaling process the gate length is changes from 80 nm to 60 nm and the operating voltage from 1.6 V to 1.2 V, the delay of the device would change from 100 ns to --------. In case if the voltage changes from 1.6 V to 1.4 V , then the scaled device would show delay as -----.

xiii. In a MOS transistor tox reduction puts more/less gate leakage current and if the thickness of tox is to increased by 5 times , then to maintain same leakage current the dielctric constant of the oxide would be ------times.

xiv. In a short channel MOS device , the carrier injection near source end is modelled as vth, this requires higher/lower channel doping near source end and needs more /less vertical electric field at that point.

xv. In a double gate Si/SiO_2 depleted SOIMOSFET with Si thickness as 8nm , the critical length would be more than ----- nm to avoid short channel effect and this critical length is more/less if the higher dielectric is used (tox as 2 nm). This critical length would be -----if the oxide permittivity is increased by 4 times.

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2. Explain different process steps to make a CMOS structure on SOI based substarate having a silicon thickness as 100nm when isolation region of NMOS and PMOS is made from the top by converting Si into SiO_2 by mentioning the oxygen dose required.. Find the critical doping required to make this into fully depleted double gate n-MOS when bottom substarte is used also as gate.

   (6)

3. A Silicon substarte doped with Boron by 1.5x $10^{15}/cm^3$ and exposed with oxygen from the top side with a dose of 2.2 x10 16/cm2 and then deposited with a metal with workfunction of 4.6 eV. Sketch and label energy band diagram across MOS structure under no bias and also when metal is biase with 0.2 Volt. Assume voltage across oxide as 0.2 under no biasing. (6)

4. Sketch and label DGSOI n-MOSFET having n+ poly as gate and SiO_2 as both oxides. The capacitances/area of forward and back oxides are 3.45x10^-7 F/cm^2 and 3.45x10^-8F/cm^2 respectively and channel doping is 10 ^16 /cm^3. Assume the Si region just gets depleted when both the gates are at inversion.

   (a) Comment on the operation of the device if Si doping is increase by 10 times also comment on forward channel behavior if back gate voltage is changed.
   (b) Comment on the role of back gate voltage variation if back gate is changing in negative polarity.
   (c) Sketch and label potential variations from top gate to bottom gate under both channels are in inversion and also when top layer is inverted but the bottom is depleted.
   (d) Compute V_T if both channels are inverted (assume oxides are charge free).
   (e) Compute subthreshold slope(S) at room temperature under full depleted case. (12)

5. A CMOS inverter has been tested to measure its delay with respect to varied load (C_L) and shows a slope of 2ps/fF. The testing results have been plotted for fanout 1 and 2 respectively to show typical dalays as 20 ps and 30 ps respectively. Estimate the typical Rsd, Cin and Cout.

   (6)
