BIRLA INSTITUTE OF TECHNOLOGY & SCIENCE, PILANI, RAJASTHAN

Second Semester 2022-2023
Comprehensive Examination (Closed Book – 40 Marks)

Course no: EEE F477 Max. Marks :80
Course Title: Modeling of Field Effect Nano Devices Weightage : 40%
Date : 11-05-2023 Duration : 180 minutes

[Relative permittivity of Si and SiO_2 as 11.8 and 3.9.ϵ_0 = 8.85x10^{-14} F/Cm, n_i= 1.5x10^10/cm^3, Eg= 1.12 eV, kT =0.026 eV all at room temp.Eg for Ga As is 1.42 eV and for Al As is 2.16 eV]

[Q1 to 6 each 6 marks and Q7 is for 4 marks]

1. In a VLSI technology, if length is scaled from 100 nm to 70 nm and voltage is scaled from 2 V to 1.5 Volt then find the scaling of the following:
   (i) x_j of the source/drain
   (ii) oxide thickness
   (iii) delay
   (iv) power

2. Discuss the role of DIBL and punch through in scaled devices and also mention suitable approach to mitigate these effects. Comment on the punch through voltage if the channel length is halved and the doping is doubled.

3. Discuss in brief the process of super steep retrograde channel engineering and halo implantation, mentioning their roles in performance parameters. How source/drain engineering is done to reduce Rs and Rd ?

4. Discuss the role of injection velocity and its relation with the thermal velocity and carrier mobility in scaled devices. In such devices suggest some solutions to avoid mobility degradation near injection point. Also comment on velocity overshoot effects in Si and GaAs based scaled devices if any.

5. Discuss the quantum confined stark effect in the design of a quantum well detector and its role in discriminating two close wavelength by 10 A^0 . Explain with a suitable structure and circuit diagram.

6. Find the suitable condition for the capacitance required and its limit towards leakage conductance for a single electron device. Estimate the size of the capacitor for a 400 mV Colombian barrier and also typical corresponding leackage current.

7. How subthreshold slope varies in scaled devices for single, double, triple and all around MOSFET , explain with reasoning ? Comment on the short channel effects in terms of natural lengths for the cases of single, double and gate around MOSFETs.

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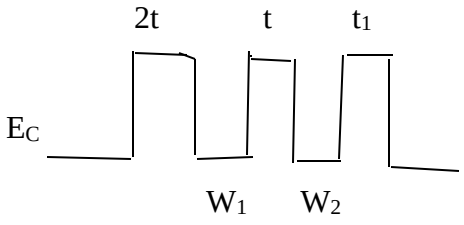
1. Sketch and label energy band diagram across metal (WF= 5 eV) , $Ga_{0.4}Al_{0.6}As$ and GaAs structure assuming $Ga_{0.4}Al_{0.6}As$ (WF = 4.8 eV) is larger n type and fully depleted under unbiased condition and GaAs is lightly doped. (electron affinity for GaAs is 4.07 eV).

2. Sketch and label the energy band diagram and two lowest quantum levels of an RTD made from GaAs/ $Ga_{0.2}Al_{0.8}As$ having a well and barrier width as 3 nm and 4 nm respectively. Assume first level in the well as 60 meV and $\Delta Ev = 0.4\ \Delta Ec$. Estimate the Vp and Ip for the RTD if the well width is reduced to 2.5 nm having positive resistance as 1 k Ω.

3. . Design a double gate MOSFET having top gate oxide thickness as 1.5 nm and bottom oxide has dielectric constant as double of the top oxide but the capacitance is 1 %. Assume silicon thickness is 40 nm and is completely depleted under inversion operation for a given channel doping of N_A. Estimate subthreshold slope (S) of the device in that case . Also comment on S value if doping is doubled

4. Design an intraband absorption based quantum detector based on GaAs/ $Ga_xAl_{(1-x)}As$ to detect photon. Assume first energy level of the quantum well is 50meV, determine the suitable wavelength to have a better responsivity.Also suggest suitable value of **x** needed to have a barrier more than thermal energy . Comment on the value of the absorbed wavelength if the well thickness is halved.

5. Use the following structure to design a quantum cascade laser to generate a 12 μm EM wave. Asssume E_1 in W_2 well has 100 meV. Show the direction of bias in the structure and find the condition for t_1 in terms of t. Also find the suitable height of the barrier.



6. Design a reduced surface LDMOS transistor to have a breakdown voltage of 400 V when the buried oxide thickness is 3 micron and breakdown field is 10^5 V/cm. Use Si/SiO_2. Comment on the breakdown voltage if a higher dielectric oxide is used .

7. .Discuss salient features of an SOI lateral bipolar transistor and its limitation. Comment on the use of a vertical SOI BJT with important design and operation improvements

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