Birla Institute of Technology & Science, Pilani, Pilani Campus
First Semester 2023-2024
EEEG512 Embedded System Design
Midterm Test (Closed Book)

Date: 14-10-2023 **Max Marks: 25** **Duration: 1 Hr 30 Min**

Note: Marks will not be awarded for Vague, unnecessarily lengthy, ambiguous answers

Q1. Multicore processors belong to- SISD, MISD, MIMD or SIMD? Choose the most appropriate answer and Justify your answer . Mention the main difference between SISD and MISD processors. Do not mention just the expansion of the abbreviation. Your understanding of the same should be reflected in the answer. **[1.5M]**

Q2. For an embedded application implemented on ARMv4 architecture based microcontroller, the following VIC initializations are made . **[3M+1.5M+1.5M]**

VICIntSelect = 0x00100000
VICIntEnable = 0x80100030
VICVectPriority20 = 0x0000000F
VICVectPriority4 = 0x00000001
VICVectPriority5 = 0x00000000
VICVectPriority31 = 0x00000000
VICSWPriorityMask = 0x0000FFFF

Bit	31	30	29	28	27	26	25	24
Symbol	I2S	I2C2	UART3	UART2	TIMER3	TIMER2	GPDMA	SD/MMC
Bit	23	22	21	20	19	18	17	16
Symbol	CAN1&2	USB	Ethernet	BOD	I2C1	AD0	EINT3	EINT2
Bit	15	14	13	12	11	10	9	8
Symbol	EINT1	EINT0	RTC	PLL	SSP1	SPI/SSP0	I2C0	PWM1
Bit	7	6	5	4	3	2	1	0
Symbol	UART1	UART0	TIMER1	TIMER0	ARMCore1	ARMCore0	-	WDT

Assuming that **prefetch abort is also raised when the VICRawIntStatus register has value =0x80100030.** [You can assume that the Vector Address Registers are initialized correctly. In CPSR both IRQ and FIQ are enabled. After this programmer does not explicitly modify F or I bit in the exception handler.]

a) Mention the order in which interrupts will be processed (started and ended) by ARMv4 architecture?

b) Why is prefetch abort handling delayed till the execution stage of the instruction raising the abort even though the abort is raised at the fetch cycle itself?

c) For an ARM 7TDMI based controller, mention at least 2 architectural reasons that make FIQ interrupt faster than IRQ interrupt?

Q.3. Assume that instructions I1, I2…I_n is executing in an out-of-order superscalar architecture… Identify all the correct statements in the list. **[2M]**

I1 I4 I5
I2 I3 ↓ *Time*

(a) The issue of the instructions can occur in the order given above
(b) The dispatch of the instructions can occur in the order given above
(c) The execution of the instructions can occur in the order given above
(d) The completion of the instructions can occur in the order given above
(e) The retirement of the instructions can occur in the order given above

Q.4. Is it possible to execute a multiply instruction and a SIMD instruction simultaneously on an ARM Cortex M4 processor?Justify your answer Interrupt jitter in a RISC processor can be lesser when compared to a CISC processor. Identify two reasons for the same. **[2.5M]**

Q.5. An engineer who recently got introduced to ARMv4 architecture was asked to write a program to implement the following. SWI call has to be raised from Thumb state, user mode. The SWI handler should check if the SWI call number is 0x10. If the number is 0x10, 8 consecutive memory locations starting from 0x40000100 should be filled with the value 0xFFFFFFFF before resuming execution of instructions from main program. If the SWI call number is not 0x010 the control should return back to main program. Program need not consider other interrupts. The register contents before and after SWI handler should be the same. The memory mapping is as follows.
Code Memory: 0x00000000-0x00008000, General Purpose RAM – 0X40000000 - 0x40001000
Stack organization: Empty Ascending , Stack memory starts from 0x40001100.

[6M]

```
                AREA RESET, CODE, READONLY
                ENTRY
                B main
                NOP
                B swi_handler
main            MOV R0, cpsr
                AND R0, R0, #0xFFFFFFD0
                MOV cpsr_c, R0
                LDR r0, =to_thumb
                BX r0
halt            B halt
swi_handler     LDM sp , {r1-r12}
                LDR R1, [R14, # -4]
                AND R1, #0x000000FF
                SUB R1, #0x10
                BNE stop1
                LDR R1, =0x40000100
                LDR R2,=0xFFFFFFFF
                MOV r0, #8
loop1           STR R2, [R1,#4]
                SUB R0, R0, #1
                BLNE loop1
                STM sp, {r1-r12}
stop1           MOV PC, LR
                code16
to_thumb        SWI 0x010
stop            B stop
                end
```

At least 12 corrections can be suggested for the program given above. Rewrite the program with minimum number of modifications to correct the program so as to meet the specifications mentioned above. Add new instructions only if the same is required to correct the program. [You are not asked to write a completely new program but to correct the above program]

Q.6. Consider a superscalar processor with 5 identical execution units. **[2M+2M+1M]**

- Instruction 1 - LDR R2, A
- Instruction 2- XOR R4,R2,R3
- Instruction 3- SUB R2,R1,R7
- Instruction 4- ADD R3, R4, R5
- Instruction 5- SUB R9,R3,R4

a. Identify all possible dependencies (and the dependency types) between instructions and suggest methods for solving dependencies.
b. For the set of instructions given above, identify if the instructions can be executed simultaneously on a superscalar architecture. Identify the order in which instructions can be issued.

c. What is speculative execution in the context of superscalar architectuers?

Q.7. Assume that you are in a brainstorming session which is aimed at selecting a processor for an embedded system which involves complex data processing operations. Choice is between processor A (CISC) and processor B (RISC). Engineer 1 says that 'A' provides 'x' MIPS while 'B' provides 'y' MIPS (y> x) and hence processor B should be used for the system. Engineer 2 argues that 'A' provides 'm' DMIPS and 'B' provides 'n' DMIPS (m > n) and hence 'A' should be used for the system.As an experienced engineer, you are required to help Engineers 1 & 2 in making the right choice of the processor. Mention your arguments for/or against the analysis of Engineer 1 and 2. If both arguments are not correct/partially correct, justify and make suggestions so as to help them make better decisions. **[2M]**

Additional Information:

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I	*F*	*T*	*M4*	*M3*	*M2*	*M1*	*M0*
						E	*A*
				GE3	GE2	GE1	GE0
N	Z	C	V	Q			*J*

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EQ	Equal	Z=1
NE	Not Equal	Z=0
CS	Carry set/Unsigned>=	C=1
CC	Carry Clear/Unsigned<	C=0
MI	Minus /Negative	N=1
PL	Plus/Positive or Zero	N=0
VS	Overflow set	O=1
VC	Overflow Clear	O=0
HI	Unsigned Clear	C=1 & Z=0
LS	Unsigned Lower or same	C=0 | Z=1
GE	Signed >=	N==V
LT	Signed <=	N!=V
GT	Signed >	Z==0,N==V
LE	Signed<=	Z==1 OR N!=V
AL	Always	

M4-M0	Mode
10000	User
10001	FIQ
10010	IRQ
10011	Supervisor
10111	Abort
11011	Undefined
11111	System