Birla Institute of Technology & Science, Pilani, Pilani Campus
I Semester 2023-2024
EEEG512 Embedded System Design
Comprehensive Examination- Part A (Closed Book)

Date:21-12-2023 **Duration: 75 minutes** **Max Marks: 15**

Note: Answers should be concise. Answer PART A and PART B on separate answer sheets only. Part A answer sheet should be submitted before starting to attempt Part B. Partial marks will not be given for Part A, so answer to the point.

Q1. How is exception exit triggered in an ARM Cortex M4 architecture ? **[1.5M]**

Q.2. While modifying GPIO port contents of a microcontroller based on RISC architecture, use of atomic operations/instructions are recommended. Write the assembly instructions required to set the Least significant bit of Port A of STM32F407IG microcontroller as an atomic write process. **[1.5M]**

Q.3.

a) An embedded system using a microcontroller(Eg: Motorola 68HC12 microcontroller) with 16 address lines has a byte addressable/organized memory. The main memory is of the maximum allowable limit. It has a direct mapped data cache, with 8 lines, with each line consisting of 16 bytes. How many bits of address are used for the tag fields? What is the size of the cache (used only for storing data)

b) In an IoT system, which utilizes cache, If we want an average memory access time of 6.5 ns, if cache access time is 5ns, and the main memory access time is 80 ns, what cache hit rate must we achieve for the cache implementation to be worthwhile?

c) Mention the steps involved in a Write back, write allocate cache when the "STR R1,[R2] " instruction is executed . Assume that the instruction cause write miss. **[1.5M+1.5M+1.5M]**

Q.4. Suppose you are developing an IoT application, which requires the microcontroller to be brought to active mode of operation from a low power mode when data is received via UART.

(a) Which of the specific low power modes of operation of the ARM CortexM4 processor can be utilized in this situation. Justify your answer.
(b) An engineer claims that WFI and WFE operates in the same manner. What is the major difference between WFI and WFE instruction ? Highlight the difference with respect to wake up from low power mode
[**1.5M+1.5M]**

Q.5. For deciding on a suitable computational unit for an wearable device which requires a DMA operation, you are considering two microcontrollers designed using AMBA AHB bus and AHB-lite bus (with multi-layer bus matrix interconnect) respectively. Both systems support DMA transfers.
(a)Based on your knowledge about AHB and AHB-lite bus architectures, comment on how the performance of both systems will differ during DMA operations.
(b)How is the arbitration process in AHB and AHB-lite bus different?.
(c)AHB-lite bus do not support split transfers. Is there is any advantage of using split transfers on an AHB-lite bus based system? Justify. [**1.5M+1M+1M]**

Q.6. What is the mode of operation of ARMv4 processor on reset.? **[1M]**
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Comprehensive Examination (Part B -Open Book)

Date: 21-12-2023 **Duration: 105 minutes** **Max Marks: 20**

Q1. You are required to establish communication between two microcontrollers on a circuit board using the SPI protocol. The master transmits the data at the rising edge of the clock. The master holds the clock line at the logical high condition when no data needs to be transmitted. What should be the CPOL and CPHA of the microcontroller which is a) master b) slave. **[1.5M]**

Q.2. a. The usable stack area for an ARMv7 processor while in privileged mode is 0x40000100-0x40000400. What should be the value stored in 0x00000000 ?
The table indicates the stack contents while in handler mode (Interrupt raised is IRQ1) . Given the following memory contents, the instruction POP {r5, r4, pc} is executed for return from exception handler for IRQ1. Assume that the exception handler and exit implementation is correct. **[1.5+1.5+1+1M]**

Memory Address	Contents
SP	0x0000_5133
SP + 04	0x4500_ffff
SP + 08	0xffff_fff9
SP + 0c	0x0000_4800
SP + 10	0x0000_5000
SP + 14	0x0000_5080
SP + 18	0x0000_0009
SP + 1c	0x0000_0087
SP + 20	0x0000_1840
SP + 24	0x0000_2380
SP + 28	0x0100_0000

b) What will be the address of instruction which will be executed after exception exit?

c) What was the mode of the processor when IRQ1 was raised?

d) If an IRQ2 (which is configured for higher priority) is raised in the system before the execution of exception return statement, which stack will be utilized for saving the context?
Note: POP is equivalent to load instruction.

Q.3. Suppose three devices which support CAN protocol attempt to transmit the messages described by the identifiers (11 bits). Device A transmits 0x223, Device B transmits 0x227 and Device C transmits 0x220.
a. If all the devices attempt to transmit simultaneously which device will be able to successfully transmit on the bus. Explain

b. If suppose Device C wants to receive only message described by identifier 0x227. How can the device C be configured to do so? Mention the two major registers in CAN controller to be configured for the same? Mention the values to be configured in the registers.

c. Suppose a data frame is transmitted by a device and the following information is available on the CAN bus (excluding the start of frame)

"01001010111100000010000……."

Assuming there are receiver nodes which can accept the message transmitted, will the transmitter or receiver detect an error for the above data? If Yes, Justify and identify the type of error. Which device will detect the error-Transmitter or receiver? **[1+1+1M]**

Q.4. You are assigned to develop a "sensor node" which is a part of a network, intended for weather monitoring in an agricultural field. Based on the sensed environmental parameters the lighting and the watering level of the field will be adjusted. The sensor node will be replicated and deployed at several parts of the field. The system specifications are as follows.

The sensor node uses STM32F407 as the microcontroller (VG or IG version). The sensor node should house solar radiation and soil humidity sensors. The sensors produce an analog output in the range 0-

3.3V. The soil humidity sensor has a resolution of 0.007 m^3/m^3 and for every 0.007 m^3/m^3 , the output changes by 13 mV. The output of solar radiation sensor is also conditioned and the resolution of the sensor is 1W/m2. For every 1W/m2 the sensor output changes by 3.3mV. The system should also have an air-temperature sensor which can be interfaced to the microcontroller using SPI protocol. Maximum clock frequency that can be provided to the temperature sensor is 5MHz. The temperature sensor provides 8-bit data as output. Refresh rate of the sensor is 50Hz. The temperature sensor module drives out data on falling edge of the clock and idle state of the clock is logic '1'. The weather conditions are to be periodically detected at intervals of 2 minutes and wirelessly transmitted to a remote monitoring unit placed at the entrance of field. The data to be transmitted has to be provided to the radio module using UART protocol at a baud rate of 115,200. The format of UART frame is as follows- 1 start bit, 8 data bits, 1 even parity bit and 1 stop bit. A push button should be made available on the sensor node which can be used to manually inspect the sensor node if the wireless data is not available from a node for certain duration of time. When the user presses the button the current value of soil humidity along with the last sensed value of other sensors will be transmitted to the remote station. [Soil humidity sensor is sampled again and the corresponding reading is transmitted where as for the other sensors the last sensed value is transmitted as the reading of other sensors will change very slowly over a duration of time].

Since, the node is battery operated, maximizing the battery life of the node is a major concern. Design the system keeping this as the priority. All the on-chip peripherals connected to APB bus should use the same APB bus (either APB1 or APB2**).In the given system, peripherals connected to only either APB1 or APB2 can be used in-addition to peripherals on AHB bus.**

Note: Marks will be awarded based on the optimal configuration of each peripheral as per the requirement. **Clearly indicate assumptions if any.**

(a) Mention, different methods by which power consumption can be minimized for the given application based on your understanding of the STM32 microcontroller. Also mention the low power modes which you will use for this application and the mode of entry and exit from the low power mode specific to this application. Clearly indicate how entry and exit from low power modes will be done.

(b) Show the clock configuration upto the PCLK2/PCLK1 configuration. You may use HSI/ HSE (HSE crystal available is 25Mhz) as the clock source. Internal PLL may be utilized. To save power consumption at what clock frequency will you run the processor, PCLK1/PCLK2. Present your analysis to show that all the requirements of peripherals are met at the selected lowest clock frequency. Estimate if the baud rate set for the UART peripheral of microcontroller is within the allowable tolerance in variation of baud rate so that the device can still receive data correctly

(c) How many interrupts will be utilized for this system design? What are the priorities of the interrupts? Clearly mention the major activates to be carried out within each interrupt service routine (NVIC config need not be mentioned).

(d) Initialize the following on-chip peripherals for the application - UART, timers, GPIOs, ADC should be initialized. **In the given system only peripherals on either APB1 or APB2 can be used in-addition to peripherals on AHB bus.**

[2.5+2.5M+1.5+4M]

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