Birla Institute of Technology and Science, Pilani

EEE G594, Advanced VLSI Devices

Comprehensive Examination, I Semester 2017-2018

Part A: CLOSED BOOK

Time: 2 h	**Max. Marks=70**	**Date: 02-12-2017**

[Given: ε_{Si} = 11.9, ε_{ox} = 3.9, ε_0 = 8.85×10^{-12} F/m, n_i(Si) = 1.5×10^{10} cm^{-3}, E_g(Si)=1.12 eV, q=1.6×10^{-19} C, k=1.38×10^{-23} $m^2kgs^{-2}k^{-1}$, T=300 K, μ_n=450 cm^2/V-s, μ_p=250 cm^2/V-s]

[1] Fig. 1 shows a M-I-S junction applied V_G voltage. Draw and label the distribution of following quantities for (i) V_G at V_T and (ii) V_G beyond V_T. **[12]**

(a) Charge [ϱ(x)]

(b) Electric field [E(x)]

(c) Potential [ψ(x)]

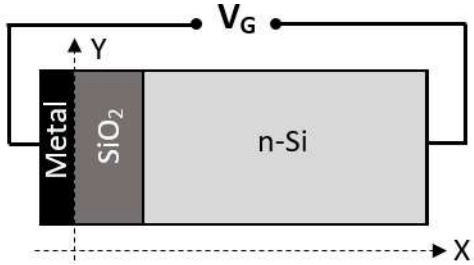

Fig. 1

[2] Consider a long channel n-MOSFET with gate width near source end is W and drain end is W+(L/a) where, L is the channel length and a (>1) is a constant. Derive a drain current expression in liner and saturation region considering gradual channel approximation approach (μ_n: Channel Mobility & C_{OX}: Oxide capacitance). **[8]**

[3] Derive an expression of electronic potential [φ(x,y)] in channel region of a fully depleted symmetric quadruple gate MOSFET considering required boundary conditions. Also derive the expression of natural length (λ) of the device from φ(x,y) expression. **[8]**

[4] (a) How electrostatic integrity (EI) varies for Bulk, FD and DG MOSFETs?

(b) How the SCE is controlled with increase of number of gate in MOSFET?

(c) What are the advantages and disadvantages of BCE and ES inverted staggered TFTs?

[4+4+4=12]

[5] (a) For an ultrathin body (t_{Si}<10 nm) DG n-MOSFET, derive the expression for channel potential considering volume inversion effect. What will be the possible change of V_T when t_{Si}<<10 nm.

(b) Describe the structural confinement (SC) and electrical confinement (EC) for FinFET? If, body doping of a FinFET increases, what confinement will be increased/decreased and why?

[6+4=10]

[6] (a) What are the origin of parasitic resistances and capacitance in FinFET source drain region (use suitable diagram)?

(b) In a double gate n-channel FinFET, source and drain region have been replaced by SiC instead of Si. What performance improvement would be found and why (use suitable diagram)?

[4+4=8]

[7] (a) How the FDSOI MOSFET reduces the static power consumption of VLSI circuit?

(b) For a SOI MOSFET, N_A=2×10^{17} cm^{-3}, t_{OX}=10 nm, t_{BOX}= 25 nm and t_{Si}= 90 nm. What is the body factor (n) of the device? If, t_{Si} reduces from 90 nm to 60 nm, what will be the new body factor (n) of the device. What is the improvement in subthreshold swing for the reduction of t_{Si}.

[4+8=12]

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Part B: OPEN BOOK

Time: 1 h	**Max. Marks=35**	**Date: 02-12-2017**

[Given: ε_{Si} = 11.9, ε_{ox} = 3.9, ε_0 = 8.85×10^{-12} F/m, n_i(Si) = 1.5×10^{10} cm^{-3}, E_g(Si)=1.12 eV, q=1.6×10^{-19} C, k=1.38×10^{-23} $m^2kgs^{-2}k^{-1}$, T=300 K, μ_n=450 cm^2/V-s, μ_p=250 cm^2/V-s]

[1] Consider an M-I-S capacitor fabricated on a p-type silicon substrate which is doped with a net acceptor concentration N_A of 2×10^{l6} cm^{-3}. The electrostatic potential of the gate metal relative to intrinsic silicon is +0.3 V and the gate dielectric is silicon dioxide of 25 nm thick. Calculate the depletion charge Q_d, inversion charge Q_i and sheet charge density in the inversion layer when the gate voltage is 2 V greater than the threshold voltage? **[12]**

[2] Fig. 1 shows a characteristics of normalized capacitance vs gate voltage (V_G) for a Metal/SiO_2/p-Si junction. If, the doping of p-Si is 5×10^{16} cm^{-3} and oxide thickness is 100 nm what is the value of normalized capacitance at point B. **[7]**

[3] Fig. 2 shows a sacrificial pattern formed by optical photolithography where P_{FIN} is 300 nm. Two step spacer defined fin formation process is applied to develop SOI FinFET. In both the steps, spacer width will be the half of sacrificial pattern width. In both the process steps, anisotropic etching time was same. **[16]**

(a) Draw the schematic of all the process steps.

(b) For tri-gate SOI FinFET formation, what will be the fin height when 40^0 tilt-angle required for S/D implant.

(c) What will be the Si wafer height (H) for the complete process steps?

(d) For double-gate SOI FinFET with same fin height in (b), what will be the hark mask height when 35^0 tilt-angle required for S/D implant.

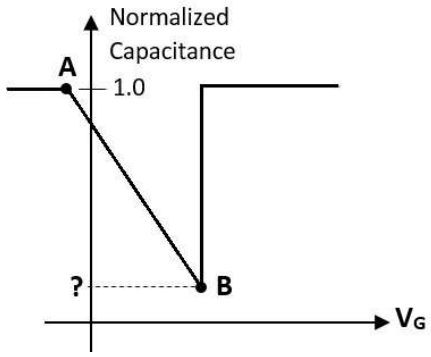

Fig. 1

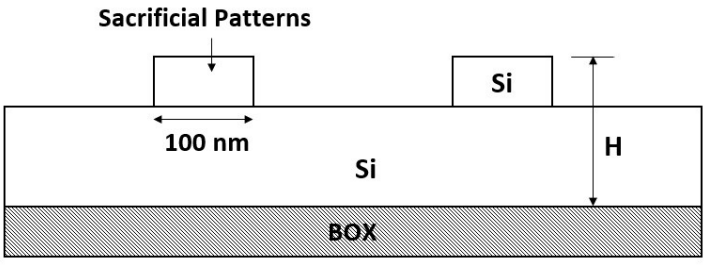

Fig. 2

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