

Birla Institute of Technology and Science, Pilani

EEE G594, Advanced VLSI Devices

Mid Semester Examination, I Semester 2017-2018

OPEN BOOK

Time: 90 min.

Max. Marks=70

Date: 09-10-2016

[Given: $\epsilon_{Si} = 11.9$, $\epsilon_{ox} = 3.9$, $\epsilon_0 = 8.85 \times 10^{-12}$ F/m, $n_i(\text{Si}) = 1.5 \times 10^{10}$ cm⁻³, $E_g(\text{Si}) = 1.12$ eV, $q = 1.6 \times 10^{-19}$ C, $k = 1.38 \times 10^{-23}$ m²kgs⁻²k⁻¹, $T = 300$ K, $\mu_n = 450$ cm²/V-s, $\mu_p = 250$ cm²/V-s]

[1] Consider a n-channel n⁺ poly-SiO₂-Si MOSFET with gate oxide thickness (t_{ox})=5 nm, channel length (L) = 0.6 μ m and acceptor impurity (N_A)= 2×10^{17} cm⁻³. Calculate V_{Dsat} value with and without gradual channel approximation considering flat band voltage (V_{FB}) -1.1 V, $V_{GS} = 2$ V and bulk to source voltage (V_{BS}) zero. Again calculate the V_{Dsat} considering velocity saturation where saturated velocity of electron at room temperature (v_s) is 10^7 cm/s. [14]

[2] For a n-channel bulk MOSFET, $t_{ox} = 5$ nm and $N_A = 2 \times 10^{17}$ cm⁻³. Also consider the threshold voltage (V_{T0}) of the device is 0.4 V, subthreshold slope 100 mV/decade and drain current 0.1 μ A at V_{T0} . What is the subthreshold leakage current at $V_{GS} = 0$ V? Also calculate the required additional back gate bias (substrate to source voltage) to reduce the leakage current by one order of magnitude. [12]

[3] For a short channel bulk n-MOSFET device $t_{ox} = 50$ nm, $N_A = 2 \times 10^{16}$ cm⁻³, $L = 0.6$ μ m, source/drain junction depth (x_j)=1 μ m, source/drain doping (N_D)= 10^{17} cm⁻³. Calculate minimum drain to source voltage (V_{DSPT}) when punch-through starts. Also, calculate the amount of DIBL using charge sharing model for $V_D^{low} = 0$ V and $V_{Supply} = V_{DSPT}$ (Consider, $V_{FB} = -1.1$ V and $V_{BS} = 0$). [20]

[4] SOI device shown in the Fig. 1 having $N_A = 2 \times 10^{17}$ cm⁻³ $Q_f/q = 5 \times 10^{11}$ cm⁻².

- (a) Calculate threshold voltage when (i) $t_{Si} = 50$ nm and (ii) $t_{Si} = 100$ nm.
 - (b) Also calculate subthreshold slope (s) for (i) $t_{Si} = 50$ nm and (ii) $t_{Si} = 100$ nm.
 - (c) Consider, SOI device with $t_{Si} = 100$ nm: At, $V_{GS} = 1$ V and $V_{DS} = 2$ V, impact-ionization starts and silicon body potential increases to 0.5 V. What is the new value of threshold voltage (V_T) and what is the increment of drain current due to new V_T . (Consider, body factor $n = 1$ and $\lambda = 0$).
- [24]

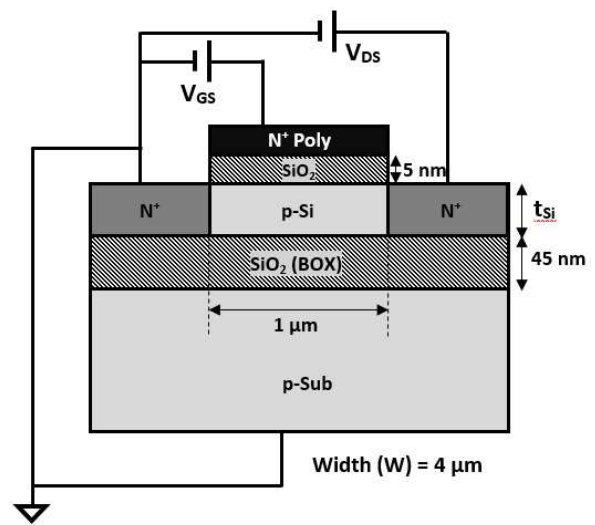


Fig. 1

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