BIRLA INSTITUTE OF TECHNOLOGY & SCIENCE, PILANI, RAJASTHAN

First Semester 2022-2023
Mid Semester Test B (Open Book) Tentative duration : 45 mins

Course no: EEE G595 — Max. Marks :60
Course Title: Nanoelectronics and Nanophotonic Tech. — Weightage : 30%
Date : 01-11-2022 — Duration : 90 minutes

ID No : --- Name : -------------------------------------

Note: Please fill the blanks with appropriate answers OR strike off the wrong words as per the question.
(This part has to be returned) 11x2 + 4x2=30

6. (i) In a MOS device subthreshold conduction slope S (mV/decade I) would be --------in case of C_d is $C_{ox}/2$ and this would be ------if the oxide thickness is halved.

 (ii) In MOS scaling the channel length is halved and channel doping is doubled, the punch through voltage would be ------times. Now if the channel length is not changed but the doping is doubled the punch through voltage would be -----times.

 (iii) A digital MOS would become short channel around ------nm of channel length if operated at (V_g-V_t) as 1.4 V and an analog MOS operates at (V_g-V_t) as 0.2 , the critical length would be ----nm (E_{sat} =10^5 V/cm)

 (iv) A conventional nMOS device with oxide thickness of 1 nm has drain drain depletion effective depth in the channel is 1% of the channel length and produces 100 mV drop in threshold valtage due to length scaling, the Q_D would be -----and this drop in V_T would be more/less visible if the drain depth is increased.

 (v) In MOS channel length scaling influence over V_t rollout is less/more, if the S/D depth is reduced. This rollout is more /less sensitive in case of increased channel doping.

 (vi) Electron generates scalar/vector field and the photon are scalar/vector field, while the surface plasmons are generated by reflection/refraction/scattering process at the metal dielectric interface.

 (vii) In a SET if QD has 1aF capacitance, the potential barrier would be ------and the required capacitor size for SET to work at room temperature would be ------------.

 (viii) In bio imaging one protien with fluorescent dye acts as donar/acceptor as bio image to another protien when comes in proximity distance of ----- and this interaction increases/decreases by a factor -----if the distance is halved.

 (ix) In a MOS device if collison time is 0.2 ps and V_{sat} is 10^7 cm/s , the ballistic model would be valid upto length of ------and if the collison time increases the velocity overshoot probability increases/decreases with the short channel length limit increased /decreased.

(x) In a double gate Si/SiO_2 depleted SOIMOSFET with Si thickness as 8nm , the critical length would be more than **-----** nm to avoid short channel effect and this critical length is more/less if the higher dielectric is used (t_{ox} as 2 nm).

(xi) Silicon MOS devices using Si_3N_4 over gate puts compression/tensile stress on channel and Ge in S/D puts compression/tensile stress on channel.

(xii) An DGSOI n-MOSFET has n+ poly as gate and SiO_2 as both the top and bottom oxide capacitances are $3.45x10^{-6}$ F/cm^2 and 3.45 $x10^{-7}$/cm^2 respectively. Under the case if both top and bottom region are in inversion , the si get depleted for acceptor doping of 10^{17}/cm^3, the thicknesses of top oxide, si and bottom oxide would be -------,------ ----and ------------ respectively. Further if the doping is increased 4 times the input impedance of the device increases/decreases.

(xiii) In a MOS scaling process the gate length is changes from 80 nm to 60 nm and the operating voltage from 1.6 V to 1.2 V, the delay of the device would change from 100 ns to -------. In case if the voltage changes from 1.6 V to 1.4 V , then the scaled device would show delay as -----.

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Mid Semester Test A (Close Book) **Tentative duration : 45 minute**

Q.1 to 5 each of 6 marks.

1. Explain different process steps to make a CMOS structure on SOI based substarate and also a conventional CMOS over p-substarte mentioning any four improvements observed in SOI case.

2. Sketch and label two barrier RTD structure made of GaAs/$Ga_{0.3}$ $Al_{0.7}$As having barrier width of 2 nm and width as 2.8 nm respectively. Assume E_1 as 100 meV and voltage drop across accumulation and depletion regions during biasing as 140mV, then compute V_p and V_v assuming PVVR as 1.4. Find the positive and negative resistances if the peak and valey currents are 100µA and 40 µA respectively. Comment on these values if the well thickness is changed to 3.2 nm. (Assume ΔE_v as 0.2 eV, Eg for GaAs and AlAs as 1.42 eV and 2.16 eV respectively)

3. Mention any four channel impairment due to short channel effects in scaled MOS devices and discuss steps to mitigate those effects in terms of channel and S/D engineeting. Comments on the S/D resistance optimization.

4. Comments over short channel effects in SOI DGMOS devices and channel length limitations in terms of silicon and oxide layer thicknesses and their permitivities. Comments on short channel limitations in case of single,double,triple and gate all around SOI MOS devices.

5. Explain conditions for an SOI DGMOSFET to operate in PD and FD mode. Sketch and label the electric field and potential from top gate to bottom gate when both are in inversion.