Q5, Assume $\Delta E_v = 0.2 \Delta E_c$

Q.3 = Ring path length is 100λ and L_c is ignored

BIRLA INSTITUTE OF TECHNOLOGY & SCIENCE, PILANI, RAJASTHAN
First Semester 2022-2023
Comprehensive Examination

Course no: EEE G595 Max. Marks :70
Course Title: Nano electr. & nano photonics Tech. (**Open-Book- 35 marks**) Weightage : 35%
Date : 21-12-2022 Duration : 3Hrs

Q1: Design a Silicon based FP based optical filter , suitable to filter 10 optical channels each separated by 200 GHz and working at 40 Gbps. How this design can be modified to accommodate such 40 channels ? **(4)**

Q.2: Design a palnar optical Silicon film based waveguide sandwitched between SiO_2 to operate in single mode at 1500nm. Now use this waveguide to make the following (mention all the used suitable design paramenters):

(i) Mode filter to allow only TE mode to pass.

(ii) Phase shifter to make π phase shift assuming inverted charge model through MOS structure which can make Δn as 5 %.

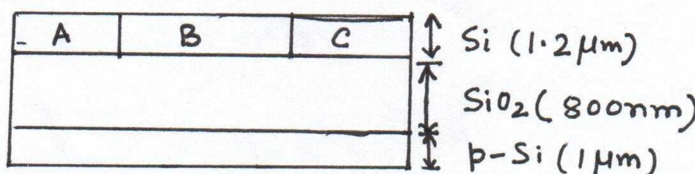
(iii) Grating to reflect 1500 nm assuming effective index of the grating is average of denser and rarer medium. **(6)**

Q3: Design a ring resonator using Si waveguide to couple 1540 nm. Extend the design to make this as a tunable ring to select varied wavelength using MOS structures which changes effective n by 5% and find the selected λ and new FSR. Assume ring resonate for path length of 100λ. **(6)**

Q4: How does current drive varies from single gate MOS,double gate MOS to FinFET devices ? Assuming 5nA current for unit width planar single gate device, estimate the drive current for a double gate, single finger FinFET and also multifinger FinFET. Assume width of single finger (W) as 30nm,silicon film thickness (t_s) as 40 nm and finger pitch(P) as 100nm. Also find drive curents if the finger pitch is changed as 50 and 150. **(6)**

Q5: Sketch and label the energy band diagram of a RTD formed by GaAs (1.42 eV) and $Ga_{0.2}Al_{0.8}As$ (Eg of AlAs as 2.16eV) with well width as 3 nm. Estimate two lower energy levels assuming effective mass of electron as 0.8 m_e. Design a RTD based circuit to realize EXOR and EXNOR gate. **(6)**

Q6: Use the given sample to make CMOS device ensuring nMOS in region A , pMOS in region C and isolation in region B. Sketch the structures to show input, output terminals of the designed CMOS. Estimate the appropriate etching depth required in region B so that it can be converted into SiO_2 by properly exposing to oxygen dose assuming Si has $5x10^{22}$ atoms/cm^3 mentioning suitable oxygen dose required.Now in another process use the same sample to make a double gate MOSFET by depositing 2 nm top oxide for top gate in such a way that region B is used for channel and regions A and C are used for Source and Drain. Compute Cox for the top and bottom oxide regions and also subthreshold slope uder full depletion DGMOSFET model of the device. **(7)**



Sample

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BIRLA INSTITUTE OF TECHNOLOGY & SCIENCE, PILANI, RAJASTHAN
First Semester 2021-2022
Comprehensive Examination

Course no: EEE G595 Max. Marks :70
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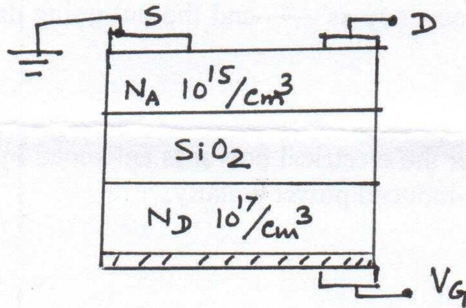
Date : 21-12-2022 Duration : 3Hrs

Note: Use following data if not given in a problem.
$\varepsilon_o = 8.86\times10^{-14}$F/cm, ε_r (SiO_2) = 3.9, ε_r (Si) =11.8, kT/q = 0.026V.
n(Si) = 3.6, n(SiO_2) = 1.5
Each question from 1 to 8 carries 4 marks and question number 9 is of 3 marks.

Q.1: Design an electrooptic MZI based modulator to implement electrical AND, OR and EXOR operation to get appropriate optical output.

Q.2: In the given structure V_G is applied to create a depletion region below SiO_2 .Find
(i) Polarity of V_G and critical thickness of region above SiO_2 to provide 4 nm channel. Comment on th polarity of D voltage to operate it in conduction mode.
(ii) When bottom region is illuminated, comment on the channel conduction .
(iii) In case the polarity of V_G is reversed , comment on the conduction under illumination.



Q.3: A Si (n=3.6) waveguide collects 16% of the incident light and operates as single mode at 1500 nm, then predict waveguide thichness and the index of the surrounding medium of the waveguide. Also calculate maximum and minimum values of the longitudinal components of the wave vector which can propagate at that wavelength.

Q4: Comment on the operating conditions of a p-n junction to operate as injection laser cavity mentioning any two important conditions. Sketch and label the energy band diagram of a double heterojunction p-n junction operating in laser mode mentioning its difference with an similar homojunction laser.

Q.5 : In a single electron transistor design, discuss any two important conditions . Estimate suitable capacitance of QD involved to operate at room temp and also corresponding tunnel current.

Q.6:How can subthreshold leakage and direct tunneling leakage current in scaled devices can be mitigated ? Sketch qualitatively thease leakage currents with respect to oxide thickness and comment their role in design od scaled MOSFET and Scaled DRAM applications.

Q.7: How does source/drain induced depletion charge influence the V_T of the short channel MOSFETs, derive a suitable expression of these shared charge to influence V_T in terms of W_m (max. depletion region below oxide), x_j (depth od S/D regions and Q_D (depletion charge below oxide) and L (channel length). Sketch and label qualitatively V_T Vs L for two values of X_{j1} and X_{j2} ($X_{j1} < X_{j2}$).

Q.8: Discuss the limitation of single QW laser and comment how can MQW laser improve the performance of laser action. Sketch the energy band diagram of a MQW laser having separate confinement heterostructure. Why and how the compressive strain in QW laser influences the threshold current ?

Q9. : Write short answers only in one or two lines for the following:

(i): Role of drift and diffusion current when the MOS devide operates above and below VT (threshold Voltage)

(ii): Role of I_{drift}/W and $I_{diffusion}/W$ constant fileld svcaling the with respect to scaling k.

(iii) In channel engineering under super steep retrograde channel the used profile and dopants to minimize dopant diffusion spread during annealing for PMOS device