BIRLA INSTITUTE OF TECHNOLOGY & SCIENCE, PILANI, RAJASTHAN

First Semester 2023-2024
Mid Semester Test A (Closed Book) Tentative duration : 45 mins

Course no: EEE G595 | Max. Marks :60
Course Title: Nanoelectronics and Nanophotonic Tech. | Weightage : 30%
Date : 10-10-2023 | Duration : 90 minutes

Note: Each part of the first question is of 3 marks, attempt any 10. Please answer in brief. [Relative permittivity of Si and SiO2 as 11.8 and 3.9.$\epsilon 0$ = 8.85x10-14 F/Cm, ni= 1.5x10^10/cm^3, Eg= 1.12 eV, kT =0.026 eV all at room temp.Eg for Ga As is 1.42 eV and for Al As is 2.16 eV]

1. (i) Find subthreshold conduction slope S (mV/decade I) for the case if C_d is 0.4 C_{ox} . Further estimate this if the oxide permittivity is increased by 4 times of SiO_2.

   (ii) In MOS scaling process the length is scaled from 90 nm to 60 nm and voltage is scaled from 1.2 V to 0.9 V. Find the current in the scaled device in terms of the original one . Further predict a suitable voltage so that the scaled current becomes 2/3 time of the original.

   (iii) Sketch and label E-k diagram for an electron and also for a photon. Comment on the wavelength of a photon and of an electron having same energy in one sentence.

   (iv) Comment on the bound energy of an exiciton in terms of the bandgap energy. Discuss the role of temperature in exciton formation with a specific example.

   (v) Sketch and label the energy band diagram across two semiconductor A (Eg=1.6 eV) and B (Eg= 1.2 eV) at room temperature. Assume $q\chi_1$ - 0.2eV = $q\chi_2$.

   (vi) A conventional nMOS device with oxide thickness of 1 nm has drain drain depletion effective depth in the channel is 1% of the channel length and produces 100 mV drop in threshold valtage due to length scaling. Predict the Q_D in terms of ϵ_{ox} and also comment on this drop if the drain depth is increased.

   (vii) If the V_T of a n+ poly gate with p-substarte doped with 1.5x10^15/cm^3 is 0.3 V, then calculate VT in case gate is made of p+ poly. Also comment if the metal work function of metal is $q\chi_{si}$ + 0.56 eV.
   (viii) Explain conditions for an SOI DGMOSFET to operate in PD and FD mode. Sketch and label the electric field and potential from top gate to bottom gate when both are in inversion.

   (ix) Find the critical length in a double gate Si/SiO_2 depleted SOIMOSFET having Si thickness as 6nm to avoid short channel effect. Comment on this critical length if silicon oxide is replace by haffnium oxide (t_{ox} as 2 nm for both the cases).

   (x) Sketch and label leakage current in a nMOS transistor for gate induced and substrate induced case with respect to gate thickness with brief explanation.

   (xi) Sketch and label the threshold voltage variation due to length scaling for two channel doping Nd_1 and Nd_2 ($Nd_1 < Nd_2$)

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Mid Semester Test B (Open Book) **Tentative duration : 45 minute**

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1. Sketch and label energy band diagram and also electric field distribution across a n+ poly Si/SiO_2/p-Si (doped with 1.5x10^16/cm^3). Assume voltage across SiO_2 is 0.2 V. Comment on the nature of Si region just below SiO_2 at Vg as 0.0 V, - 0.5 V and +0.5 V respectively. (6)

2. Sketch and label DGSOI n-MOSFET having n+ poly as gate and SiO_2 as both oxides. The capacitances/area of forward and back oxides are 3.45x10^-6 F/cm^2 and 3.45x10^-7 F/cm^2 respectively and channel doping is 10 ^15 /cm^3. Assume the Si region just gets depleted when both the gates are at inversion.

   (a) Comment on the operation of the device if Si doping is increase by 4 times also comment ofn forward channel behavior if back gate voltage is changed.
   (b) Comment on the role of back gate voltage variation if back gate is changing in negative polarity.
   (c) Sketch and label potential variations from top gate to bottom gate under both channels are in inversion.
   (d) Compute V_T if both channels are inverted (assume oxides are charge free).
   (e) Compute subthreshold slope(S) at room temperature under full depleted case. (12)

3. Mention any four channel impairment due to short channel effects in scaled MOS devices and discuss steps to mitigate those effects in terms of channel and S/D engineeting. Comments on the S/D resistance optimization. (6)

4. A nMOS transistor operates in subthreshold condition in such a way that surface potential at source end is 100mV. Compute the electron concentration at the source end and drain end for a channel of 100nm when drain operates at 0.9 V. Also compute the diffusion current if any in the channel and S (mV/decade I)at room temperature assuming Cd as 0.5 of Cox. (6)