Please read all questions carefully. Answer in as much detail as asked for.

Q 1. Answer the following [6 marks]
  a. What are the advantages of hardware/software co-design approach over a traditional design approach? What are the driving factors in hardware/ software co-design?   [2 + 1]
  b. Discuss in detail the generic co-design methodology (i.e. the steps involved in co-design) [3]

Q 2. Answer the following [6 marks]
  a. Describe four benefits/purposes of having an abstract HW/SW model?   [2]
  b. What does abstraction mean in the context of system model? What are the three different abstraction levels at which a system can be modeled? [0.5 + 1.5]
  c. Name any three 'Unified HW/SW representations' using which the system can be modeled at high level? Give example of any one of them?   [2]

  3. Answer the following [9 marks]
  a. Describe in detail Hardware/Software Partitioning and the constraints driving the same. [3] What are the different issues to be accounted while doing the partitioning [2].
  b. Given a system to be partitioned with the following constraints, mathematically formulate a suitable objective function which can be used to evaluate a partition's suitability over others: [3]
     Area (A) < 10 cm^2
     Delay (D) < 5 ms
     Power consumption (P) < 3 mW
     Cost (C) < \$10
  c. Mention one advantage and one dis-advantage of using greedy algorithms for HW/SW partitioning. [1]

 4. Differentiation between the following giving suitable examples [2+ 2+ 2 = 6 marks]
       a. Informal functional specification and Refined functional specification [2]
       b. Software-oriented partitioning and Hardware oriented partitioning [2]
       c. Coarse granularity and Fine granularity in context of HW/SW partitioning [2]


  5. Answer the following [2+2+2= 6 marks]
  6. Define Hardware Synthesis and Software Synthesis and mention its benefit [2].
  a. Draw the schematic diagram of Sanders Co-design methodology [2].
  b. List any 4 major co-design tools developed based on university research. [2].

6. Consider the following Data flow graph, architecture graph and the additional details. X, Y and Z are the inputs to the system and O is the output. Note that F1, F2, F3 and F4 are functions whereas C1, C2 and C3 are communication processes. The additional details describe the time a particular function/process takes to be executed on a particular component (Note HWM refers to Hardware module).   [3+3+3+3= 12 marks]

X   Y   Z
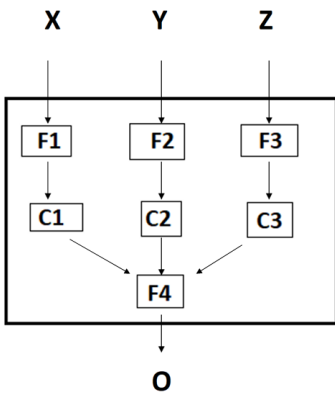
Application DFG
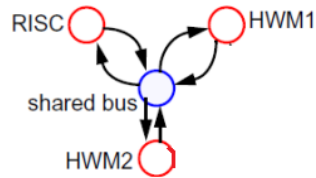
Architecture graph

Function / Process	Componet	Time taken (ms)
F1	RISC	9
F1	HWM2	3
F2	RISC	6
F2	HWM2	4.5
F3	RISC	9
F3	HWM2	3
F4	RISC	12
F4	HWM1	9
F4	HWM2	6
C1	SB	~0
C2	SB	~0
C3	SB	~0

Additional details

a. Draw the specification graph for the given problem.   [3]
b. Draw the implementation graph given that the system is supposed to generate the output within a time deadline of 12 ms.
   Clearly highlight (/draw) the i. feasible allocation [3]
                                        ii. feasible binding. [3]
                                        iii. Scheduling of the different tasks/functions [3]

7. Consider the following model [5 marks]
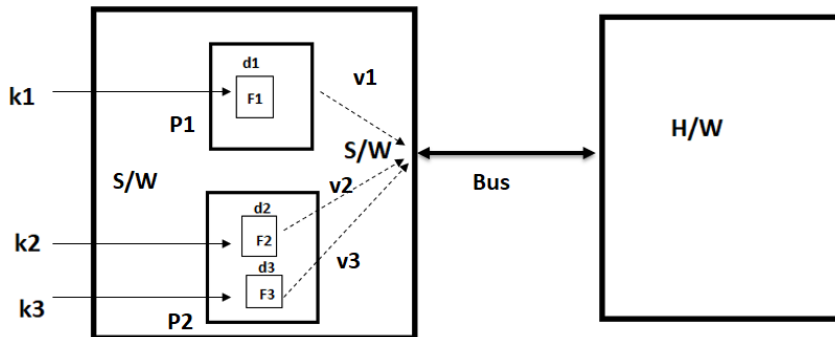
There are two processors in the s/w partition (P1 and P2) where function F1 is implemented in P1 and functions F2 and F3 in processor P2. k1, k2 and k3 denote the task arrival rates at the respective processors as shown in the figure above and d1, d2 and d3 denotes the execution delay for the task processing at the processors respectively. There is a common bus which connects the s/w and h/w partitions and the variables evaluated after execution of F1, F2 and F3 are transferred over to the h/w partition (v1, v2 and v3). Note that these variable transfer requests arrive at the bus junction (which connects s/w to h/w partition) after 3/10 s, 3/5 s and 4/3 s respectively. Further the numerical values of the other parameters are as follows: k1=5 requests per second, k2= 2 requests per second and k3= 1 request per second. Furthermore, d1, d2 and d3 are 1/10 seconds, 1/10 seconds and 1/3 seconds respectively. Calculate the following
   a. Processor utilization of processors P1 and P2 [3].
   b. Bus utilization [2].