BITS – PILANI K.K. BIRLA GOA CAMPUS

First Semester 2019-2020
EEE G626-Hardware/Software Codesign
Comprehensive Exam: Regular (Closed Book)
Duration: 180 min Max. Marks: 35

Instructions: Make suitable assumptions and justify if required.

Q1. Which is more important in an embedded computer system: throughput or latency? Explain your answer? **[01]**

Q2. List at least 3 advantages of implementing selected portions of a design in hardware, and at least 3 advantages of implementing the remaining portions of the design in software **[02]**

Q3. List the advantages of Microprogrammed control over FSM based control in hardware **[02]**

Q4. What are mail boxes? Explain its merits and demerits as a hardware-software interface **[02]**

Q5. Explain briefly hierarchical clustering partitioning algorithm with an example **[02]**

Q6. Consider another SDF graph in figure-1

a) Write down the incidence matrix. Use columns to represent nodes and rows to represent edges. How can we infer the existence of a periodic admissible sequential schedule (PASS) based on the rank of the incidence matrix?
b) Show the number of invocations for each node in 1 cycle of the schedule.
c) Find the initial number of elements in each edge buffer for your PASS schedule
d) Find the minimum size required of each edge buffer. **[08]**

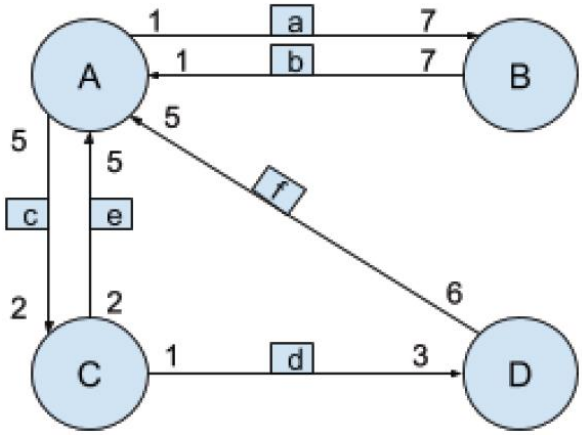

Figure-1

Q7. Retime the DFG in figure-2 such that the 3-unfolded version of the retimed DFG will achieve a critical path of 4 ut. Assume that + and X require 1 and 2 ut, respectively. **[04]**

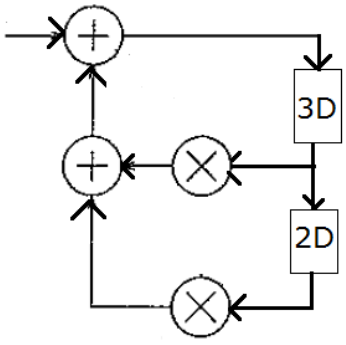

Figure-2

Q8. Design a datapath and Control path in hardware for the model given below. Allocate registers and operators. Indicate control inputs required by the data-path, and condition flags generated by the datapath. **[08]**

```
unsigned char mysqrt(unsigned int N) {
unsigned int x,j;
x = 0;
for(j= 1<<7; j != 0; j>>1) {
x = x + j;
if( x*x > N)
x = x - j;
}
return x;
}
```

Q9. You are designing a bus based accelerated system (memory mapped) that performs the following function as its main task:

```
for (i = 0; i < M; i++)
 for (j = 0; j < N; j++) {
MAXVAL = max_of_5 (pix[i][j - 1], pix[i - 1][j], pix[i][j], pix[i
   + 1][j], pix[i][j + 1]) ;
 f[i][j] = (pix[i][j - 1] + pix[i - 1][j] + pix[i][j] + pix[i +
   1][j] + pix[i][j + 1])/(5*MAXVAL);
 }
```

Assume that the accelerator has the entire ***pix*** and ***f*** arrays in its internal memory. During the entire computation of ***pix*** data is read into the accelerator before the operations begin and ***f*** is written out after all computations have been completed.

a) Show a system schedule for the host, accelerator, and bus assuming that the accelerator is inactive during all data transfers. (All data are sent to the accelerator before it starts and data are read from the accelerator after the computations are finished.)

b) Show a system schedule for the host, accelerator, and bus assuming that the accelerator has enough memory for two ***pix*** and ***f*** arrays and that the host can transfer data for one set of computations while another set is being computed.

c) Compare and contrast a co-processor based accelerator and a bus based accelerator, elaborate using the above example. **[06]**