BIRLA INSTITUTE OF TECHNOLOGY & SCIENCE, PILANI - K. K. BIRLA GOA CAMPUS

FIRST SEMESTER, 2019-2020

MID-SEMESTER EXAMINATION, VLSI DESIGN (MEL G621)

Closed Book **Maximum Marks: 40 (20% weightage)** **Duration : 90 Minutes** **Date 28.09.2019**

Q1. Consider the CMOS inverter with following parameters:

nMOS $V_{T0,n} = 0.6V$ $\mu_n C_{ox} = 60\mu A/V^2$

pMOS $V_{T0,p} = -0.7V$ $\mu_p C_{ox} = 25\mu A/V^2$

The power supply voltage is $V_{DD} = 3.3V$. The channel length of both transistors is $L_n = L_p = 0.8\mu m$.

(a) Determine the (W_n/W_p) ratio so that the switching threshold voltage of the circuit is $V_{th} = 1.4V$.

(b) The CMOS fabrication process used to manufacture this inverter allows a variation of the $V_{T0,n}$ value by $\pm 15\%$ around its nominal value, and a variation of the $V_{T0,p}$ value by $\pm 20\%$ around its nominal value. Assuming that all other parameters (such as μ_n, μ_p,C_{ox}, W_n, W_p) always retain their nominal values, find the upper and lower limits of the switching threshold voltage (V_{th}) of this circuit. **(Marks:2+4)**

Q2. An nMOS transistor is fabricated with the following physical parameters:

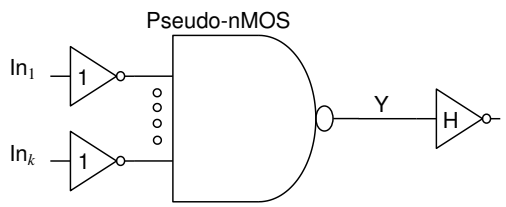
- $N_D = 10^{20} cm^{-3}$
- $N_A(substrate) = 10^{16} cm^{-3}$
- $N_A^+(channelstop) = 10^{19} cm^{-3}$
- $W = 10\ \mu m$
- $Y = 5\ \mu m$
- $L = 1.5\ \mu m$
- $L_D = 0.25\ \mu m$
- $x_j = 0.4\ \mu m$

(a) Determine the drain diffusion capacitance for $V_{DB} = 5\ V$ and $2.5V$

(b) Calculate the overlap capacitance between gate and drain for an oxide thickness of $t_{ox} = 200\ \mathring{A}$. **(Marks:6+3)**

Given : $\varepsilon_{ox} = 3.9 \times 8.85 \times 10^{-14} F/cm$, $\varepsilon_{Si} = 11.7 \times 8.85 \times 10^{-14} F/cm$, $q = 1.6 \times 10^{-19} C$, $kT/q = 0.026\ V$, $n_i = 1.45 \times 10^{10}\ cm^{-3}$

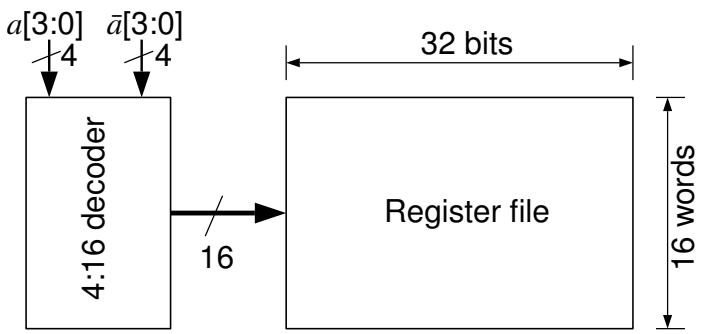
Q3. Design a k-input OR gate with DeMorgan's law using static CMOS inverters followed by a k-input pseudo-nMOS NAND, as shown in Figure below. Let each inverter be unit-sized. If the output load is an inverter of size H, determine the best transistor sizes in the NAND gate and estimate the average delay of the path.



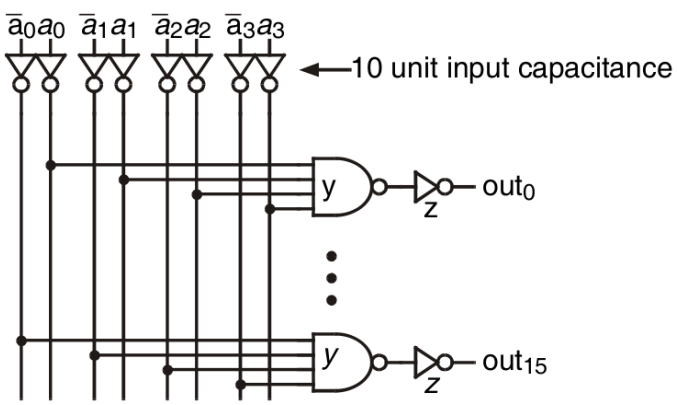
(Marks:7)

Q4. A decoder has to be designed for a register file in the embedded processor for automotive applications.The block level diagram is given below. The decoder has following specifications.

- 16 word register file.
- Each word is 32 bits wide.
- Each bit presents a load of 3 unit-sized transistors.
- True and complementary inputs of address bits a[3:0] are available.
- Each input may drive 10 unit-sized transistors.



The decoder structure is given below.



The designer needs to decide:

(a) How many stages to use?

(b) How large should each gate be?

(c) How fast can the decoder operate? (Approximate results to lower and upper integers for number of stages and do calculations for both cases).

Help the designer with answers to these question with proper supporting arguments. **(Marks:4+4+4)**

Q5. Design domino buffer with input capacitance of 3 units and load capacitance of 54 units. What will be delay of this gate? Assume size of pMOS is equal to that of size of nMOS for dynamic gate. **(Marks:6)**