BIRLA INSTITUTE OF TECHNOLOGY AND SCIENCE, PILANI, K.K. BIRLA GOA CAMPUS
FIRST SEMESTER (2022-23), END-SEMESTER EXAMINATION
VLSI DESIGN (MEL G621)

Date:30/12/2022 **Time: 180 minutes** **Total Marks: 40** **closed Book**

Instructions:

- Answer all the questions in clear handwriting. Use PEN only.
- Write all the subsection parts of a question together.

1. What is energy delay product (EDP) of CMOS Inverter? Derive the optimum value of supply voltage (V_{DD}) for which the EDP is minimized. (consider the devices are velocity saturated).

(4)

2. Calculate the transistor drain current in the following circuit as shown in Fig. 1. Assume the velocity saturated transistors with the following parameters: V_{T0} = 0.4 V, critical field E_C = 6x10^4 V/cm, W= 400 nm, L= 100 nm, V_{SAT} = 8x10^6 cm/sec, C_{ox} = 1.6 µF/cm^2, μ_n = 270 cm^2/V-s, $2|\Phi_F| = 0.88\ V$, λ = 0.7 V^{-1}, $\gamma = 0.2\ V^{0.5}$. Substrate is grounded to 0 V. consider body effect and channel length modulation effect.

(4)

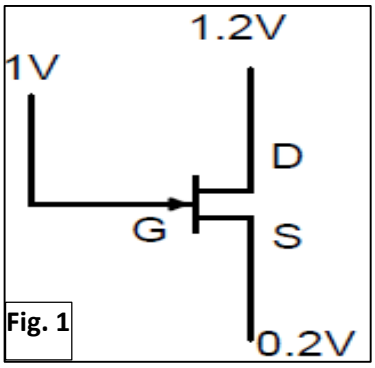


Fig. 1

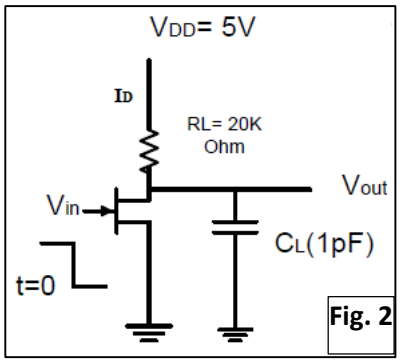
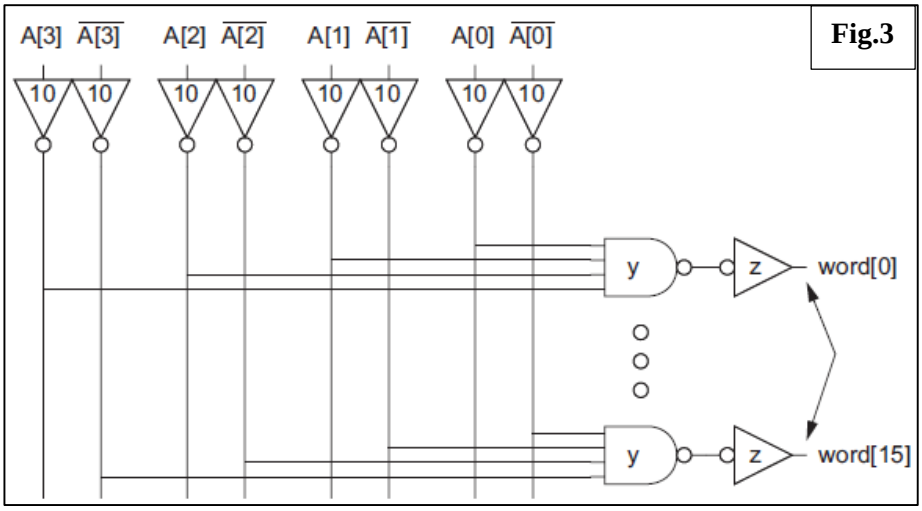


Fig. 2

3. Initially, the load capacitance C_L is discharged as shown in Fig. 2. R_L = 20 KΩ, $\mu_n C_{OX}$ = 20 µA/V^2, W/L = 15, V_{T0} = 1 V. The gate of NMOS transistor is driven by a rectangular pulse (as shown in the figure which changes from high to low delay time at t = 0). Calculate the V_{OL} and the propagation delay low to high (τ_{PLH}) for the resistive inverter logic circuit (hint: use differential equation).

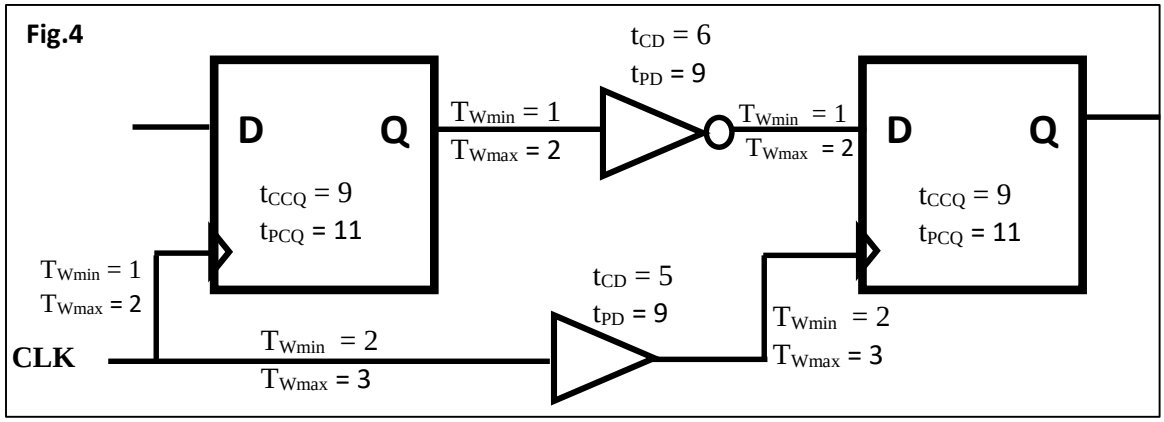
(3+5)

4. Suppose you want to design a decoder (Fig. 3) for a register file. The decoder has to drive 16 word register file with 32 bit/word. Each register bit represents a load of three unit sized transistors on word line. The true and complementary of the input address lines (A(0), $\overline{A(0)}$, B(0), $\overline{B(0)}$ etc) are available. Each address input can drive 10 unit-sized transistors.
   (i) Calculate the minimum delay (in units) and the corresponding sizes of each gate for this minimum delay of the decoder logic implementation(INV-NAND4-INV) circuit as shown below.
   (ii) How much optimum minimum delay can be achieved by only buffer insertion in the below decoder logic circuit? Find the corresponding sizes of all the gates after insertion. (ignore the logic inversion/non-inversion at the output signal due to the insertion). (5+5)

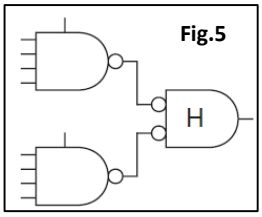


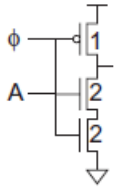
5. For the following sequential circuit as shown in Fig. 4,
   (i) What should be the minimum clock period so that there should not be any setup time violation. (both flops are identical with thold= 2 ns and tsetup= 4 ns). The T_{Wmin} and T_{Wmax} are the wire minimum and maximum delay in ns, respectively. Your answer must be justified based on the calculations.
   (ii) Also check if there is any hold time violation in the circuit implementation. If any violation exits, how can you rectify this problem in the circuit.

(3+3)



6. What is C^2MOS Latch? Explain the racing over characteristics of flop designed by this C^2MOS Latch at sampling and non-sampling edge clock overlap region. (5)
7. Suppose, you have designed a 8 input domino AND gate using footed dynamic gates and Hi-skewed NOR CMOS as shown in Fig. 5. Calculate the minimum delay for path electrical effort of 20. (for reference, you can use the footed domino inverter as shown below.) (3)





Footed domino Inverter