BIRLA INSTITUTE OF TECHNOLOGY AND SCIENCE, PILANI, K.K. BIRLA GOA CAMPUS
FIRST SEMESTER (2022-23), MID-SEMESTER EXAMINATION
VLSI DESIGN (MEL G621)

Date:4/11/2022 **Time: 90 minutes** **Total Marks: 25** **closed Book**

Instructions:

- Answer all the questions.
- Write all the subsection parts of a question together.

1. Consider a CMOS inverter with V_{DD}= 1.2 V, V_{Tn} = 0.48 V, V_{Tp} = - 0.46 V, $K_n = 982\ \mu A/V^2$, $K_P = 653\ \mu A/V^2$. Calculate the critical voltages (V_{OH}, V_{OL}, V_{IH} and V_{IL}) on the VTC and also calculate NM_L and NM_H. Ignore L-diffusion, body effect and channel length modulation in drain current equation. Devices are not velocity saturated.

(1+1+2+2+2)

2. Consider a two input NOR2 CMOS logic gate, one input is critical (time critical) between the two inputs of gate.
   (a) Draw the CMOS logic diagram indicating the critical and non-critical input signal to reduce the propagation delay. Justify your answer.
   (b) How can you reduce the logical effort for the critical input signal keeping overall pull-up and pull-down driving strength same? Design the gate sizes for the same requirement. Calculate the Logical efforts for both the inputs for low to high output transition for this gate size. (Consider the size of unit inverter is 2/1. Resistance and gate capacitance of unit transistor are R and C, respectively.)
   (c) Derive the best (minimum) and worst (maximum) low to high parasitic delay using Elmore delay model for the above NOR2 CMOS logic designed in part (b). (help: Add the junction diffusion capacitances for two different sizes of NMOS/PMOS transistors)

(2+3+3)

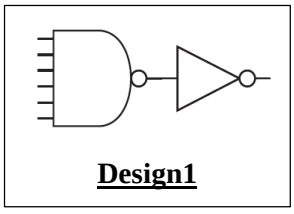
3. In a velocity saturated enhancement type n-channel MOSFET, show that $V_{DSAT} = \frac{V_C V_{GT}}{V_C + V_{GT}}$

   Here, critical voltage from drain to source is $V_C = E_C L$ and overdrive voltage is V_{GT}.

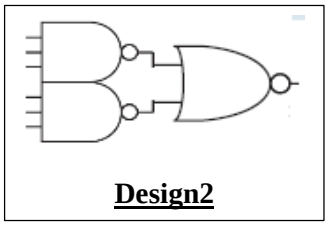
(3)

4. Consider three designs of a 6 input AND gate as shown in the below given figures. If the path electrical effort is H, then which design will be the fastest for H=1 and H= 20? Justify your answer based on the calculated delays.

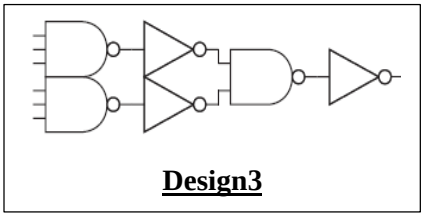
(2+2)



Design1



Design2



Design3

5. Derive the expression of worst case Elmore parasitic delay (t_{pdf}) of n-input NAND CMOS logic gate. (consider the size of unit inverter is 2/1. The resistance and gate capacitance of Unit size transistor are R and C, respectively.)

(2)