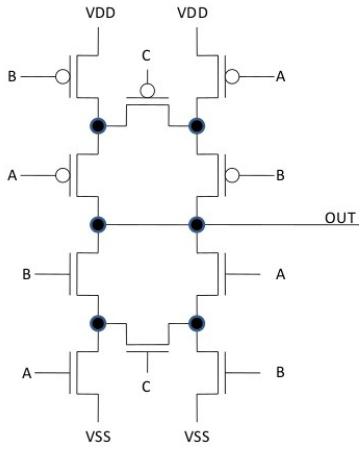
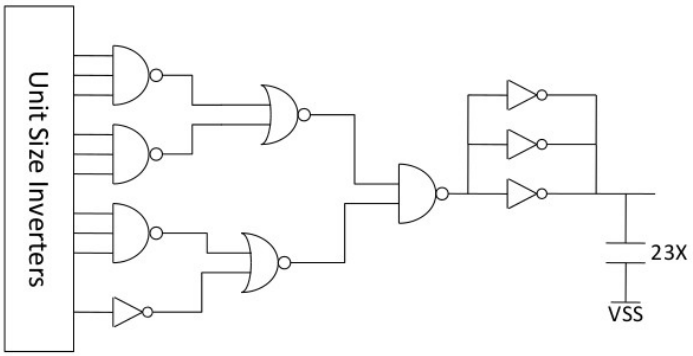
BIRLA INSTITUTE OF TECHNOLOGY AND SCIENCE, PILANII SEMESTER 2023-2024
MEL G621 VLSI DESIGN
Mid-Semester Exam: (OPEN BOOK)
M.M:60 **DURATION: 90 MIN** **14-10-2023**

Q1. Consider the CMOS inverter circuit covered in the class. Assume fabrication process with the following device parameters: V_{DD} =3V, $\mu_n C_{ox}$ =180μA/V^2 , Vt_n=0.8V, Vt_p=0.8V, $\mu_p C_{ox}$=60μA/V^2
a). Determine the size of pullup and pull down path to get the symmetric response.
b.) Assume a load capacitance of 100fF and equivalent resistance for NMOS is Rn =62kΩ & PMOS is Rp =180kΩ for unit transistors (W=1). Now, calculate the propagation delay of the circuit using RC delay method.
c). Also, calculate the propagation delay of the circuit using average current method.
d). Compare both of the delays obtained in part b & part c and comment on the difference in delay if any.

Q2. Consider the circuit shown in figure.
a). Now, draw the truth table for the output.
b). Write the boolean expression at OUT.
c). Determine the sizes of the equivalent pull up and pull down network for best case response.
Assume $(W/L)_{NMOS}$ =8, $(W/L)_{PMOS}$ =16.



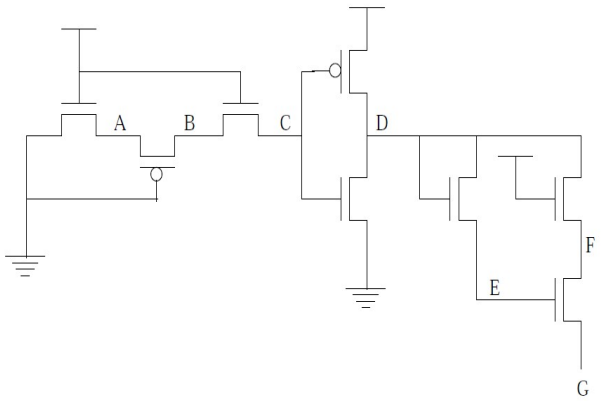
Q3. Consider the logic network shown in figure1. Assume that the network is driven by unit size inverters and the output is driving a load of 23 unit size inverters. Now, use method of logical effort and
a). Calculate the path effort.
b). Also, calculate the stage effort and calculate the delay of the path
c). Now, compute the best number of stages and the delay of the path and compare it with part b.
d). Now, compute the delay of the path using method of logical effort.
e). Finally calculate the sizes of the logic gates at each stage. (assume L=180nm, Cox=1fF, $\mu_n = 3\mu_p$).



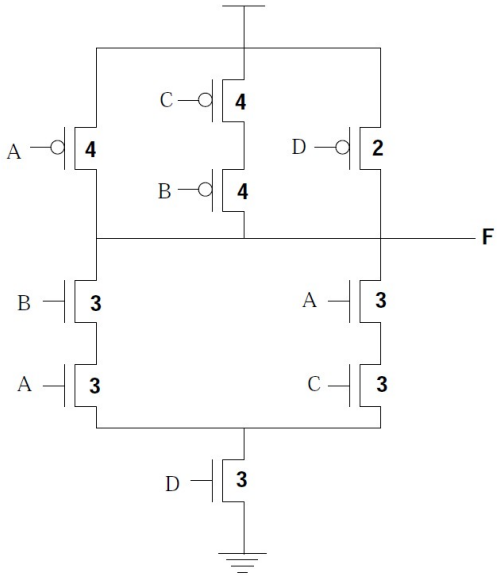
Q4. Consider the circuit shown in figure1. Now, calculate the voltages at node A, B, C, D, E, F, G in the following circuits. Assuming that the initial voltage on each node is 1.5 volts and the other circuit parameters are, Vdd =3V , Vtn = 0.5V and |Vtp| = 0.7V. Draw & write your results as shown in table1.

Table 1

Node	Voltage
Node A	
Node B	
Node C	
.....	
Node G	



Q5. Consider the circuit shown in figure1 and calcuate the logical effort for the inputs A, B, C, D



Q6. Consider a CMOS inverter with the following parameters: V_{DD}=2.5 V, Lmin=250nm, (W/L)m,min= (W/L)p,min, V_{T0N}=0.4V, V_{T0P} = -0.4V, $\mu_n C_{ox}$ = 120 uA/ V^2, $\mu_p C_{ox}$= 40 µA/ V^2 ,V_{OH} = V_{DD}, V_{OL}= 0V, V_M = 1.1V.

a). Determine the width of transistor in pullup and pulldown network. Assume the minimum width of transistor is 1µm.

b). Now, suppose due to inaccuracies in fabrication process a parasitic resistance, Rpara= 0.01 MΩ gets created in parallel to PMOS transistor. Identify whether circuit operates properly or there will be functional problem. Identify whether there will be any effect on the noise margin ? If yes, then calculate the relevant parameter and modified noise margin.

c). Now, consider case2 where due to inaccuracies in fabrication process a parasitic resistance R_{para} gets created in parallel to NMOS transistor only (Ignore partb)?

Identify whether there will be any funtional error due to this resistance and analyze its effect on the noise margin? Justify your answer.

Q7. a). Design a complete single stage static CMOS gate that implements the pull up network as given below:

PULL UP NETWORK =A'B' +C'(D'+E')

b). Draw stick diagram for the complete gate.

c). Now, draw a labeled layout of the above gate (Note: Label each layer and Ignore Design rules)