Q1. Draw neat & clean circuit level implementation for the function using static CMOS topology.

$$\textbf{Out} = \overline{[(A \cdot B) + (C \cdot D) + (A \cdot D \cdot (E + F))]}$$

Assuming that for this technology $R_p = (1/3) * R_N$

a). Now, size your gate such that the worst-case pull up resistance is equal to the worst-case pull-down resistance, assuming that the minimum transistor width is 1.

b). Now determine the worst case propagation delay assuming load capacitance of 50fF and equivalent resistance for NMOS is R_n =180kΩ & R_p =60kΩ for unit transistors (W=1).

c). Also, calculate the logical effort of this gate from the A, C and E inputs?

d). Now find out the euler path if exists and draw a labelled neat and clean layout(optimized for area) of the entire circuit   **[10]**

Q2. A 2-Input NAND gate is designed as a universal gate to implement complex boolean functions using minimum size transistors, $Vt_n = |Vt_p| = 0.6V$ and $V_{DD} = 3.3V$. Suppose the $K_n = 0.2mA/V^2$ for the pullup equivalent of the NAND gate and $K_p = 0.1mA/V^2$ for pull down equivalent of NAND gate.

a). Now, determine the switching threshold voltage V_M of NAND gate.

b). Calculate the equivalent resistance for each transistor of this equivalent inverter (using our general expression for MOSFET resistance in saturation or at edge of saturation).

c). Now, use RC delay model to calculate the rise and fall times of this circuit if the parasitic capacitance at the output is 12 fF.

d). Also calculate the propagation delay for this circuit if a load capacitances of 22fF is added at the output (use RC delay model)?

e). Now, use the inverter equivalent of NAND gate and design a ring oscillator (11-stages). Determine the frequency of operation of ring oscillator. Also determine the dynamic power consumption of a single cmos inverter stage for given (load+parasitic) capacitance driven by it.

                                                                                                     [10]

Q3. Draw a labelled NOR based 4 x 6-bit ROM circuit to store the following set of information at each of the rows.   **[8]**

a). Row1 (Word 1): 010101

b). Row2 (Word 2): 011001

c). Row3 (Word 3): 100101

d). Row4 (Word 4): 101010

Q4. A CMOS memory cell uses one nMOS access transistor and a storage capacitor to save data.

a). What type of memory is this?

b). If the nMOS access transistor has Vtn=0.6V and $\mu n = 500cm^2/V$, what is the maximum voltage that can be stored with V_{DD}=3V?

c). Assume $1x10^{-13}$ coulombs of charge are stored on this cell at a max storage voltage = 2.5V. If the minimum cell readout voltage is 0.5V, what is the maximum allowable leakage current for a hold time of 1μsec ?

d). If the minimum voltage after charge leakage on the cells is 1V, what is the final bit line voltage if Cs = 30fF (capacitor) and Cbit = 0.27pF?   **[8]**

Q5. Assume that your entire M.E batch has worked on a new process technology and developed standard cells (for all gates and blocks) having an average switiching capacitance of **120pF/mm²** and operating at V_{DD} **=0.9V.** Being an ASIC design engineer you are going to synthesize a sub-system using these standard cell with an average activity factor of **0.1**. Now, estimate the dynamic

power consumption of your sub-system if it acquires an area of **60mm²** and operates at a frequency of **400MHz.** **[4]**

Q6. Consider the circuit shown in **Figure 5.**
a). Analyze it for the following cases by assuming the initial state of Q=1 & Q'=0.
1. When D=0 & Clk=0, what is the value of Q and Q'
2. When D=0 & Clk=1, what is the value of Q and Q'
3. When D=1 & Clk=0, what is the value of Q and Q'
4. When D=1 & Clk=1, what is the value of Q and Q'
b). Now, assume case 1 and find whether there is a possibility of charge sharing or not at the output of first stage (node X & node X1). If Yes, then calcuate the effect of charge sharing on the output node voltage.
c). Find out whether the circuit is working as a level triggered or edge(positive/negative) triggered circut. **[10]**
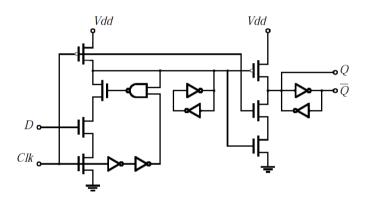

Figure 5.

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