BIRLA INSTITUTE OF TECHNOLOGY AND SCIENCE, PILANI, RAJASTHAN
I SEMESTER, 2016-2017
COMPREHENSIVE EXAMINATION
CLOSED BOOK (12 December. 2015) AN
MEL G623 ADVANCED VLSI DESIGN

TIME-3 hrs. **MAX. MARKS=35**

NOTE: state your assumptions clearly

- *Answers should be clear, concise and legible. Specify your assumptions clearly.*
- *Do all parts of same question together. Diagrams should be neat and labeled properly.*
- *NO MARKS for unnecessary theoretical explanation.*
- *Although your answers are important, your REASONS for giving those answers are even more important. Please, explain what you are doing and why. So,* ***justify your answers***

Given $g_{inv}=1$, $p_{inv}=1$, for CMOS inverter with equal delays

Unless specified in question itself, *take* --

- $u_n=3\ u_{p,,}$ Vdd=2.5 V, |Vtn|= |Vtp|= 0.5V, $W_{min}=L_{min}$= 250 nm , Υ=0, $u_n cox$=120 uA/V^2, $u_p cox$= 40 uA/ V^2
- Gate capacitance: *Cox* (NMOS) = *Cox* (PMOS) = 6 fF/um^2,
- Characteristic impedance Zo= 60 Ω , velocity of electromagnetic wave in wire **v** = 15 cm/nsec
- For $(W/L= 1)$, on-resistances of NMOS and PMOS transistors equal 13 k Ω and 39 k Ω, respectively

250 nm technology for all questions, unless specified in question itself.

Q1. An external clock is routed to two nodes X and Y through the path as shown in fig 1a. The final loads (as annotated on the Fig 1a) is a function of the unit capacitance *Cu*, which is the input capacitance of the first buffer (b1), and is equal to the input capacitance of a minimum-sized inverter

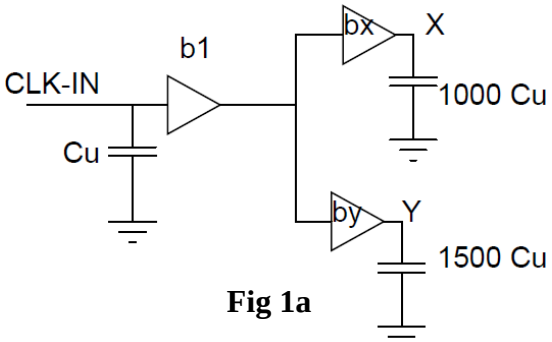

Fig 1a

a) Design the buffer **bx,** and **by** (number of stages , and capacitive load for each stage only) with minimum possible propagation delay from *Clk-in* such that the clock skew between the clock signals at X and Y is ≤. |150ps|. Assume ideal input clock. and τ for 250 nm technology is 50ps

b) Now, the clock driver circuit shown in fig 1b is used to replace every stage in the buffers **b1, bx,** and **by** of Fig 1a. Determine the value of voltage Vx (highest and lowest both) received at node X, Y.

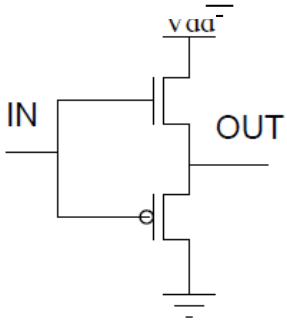

Fig 1b

c) Given, buffer **b1** is implemented by circuit of Fig. 1b. Now design the schematic of a low swing inverting clock driver which be used for stages of **bx**, and which can be driven by **b1** and gives valid signal at node X . Determine the logical effort of this low swing inverting clock driver.

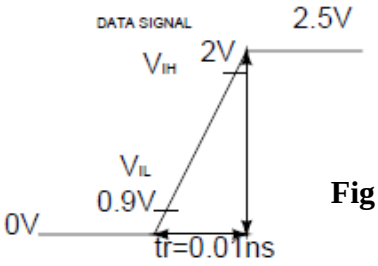

Fig 1c

d) In an SOC, 10 identical synchronizers are designed to communicate 10 bit data signal (shown in Fig 1c) from one subsystem operating at frequency F1=10 M Hz, to another subsystem operating at frequency F2=10 G Hz. It is desired to latch the data signal in one time period of F2. Calculate the value of mean time between failure ***MTBF*** if the time constant $\boldsymbol{\tau}$ of bi-stable element of synchronizer is 80ps. Also calculate the time duration of metastability window of synchronizer

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Q2. For Fig. 2, a voltage signal (0-2.5V) propagates from node A to B.

Assume the behavior of the wire (15 cm length) as lossless transmission line. Given Zo = 60 Ω, Z_T = 1 kΩ

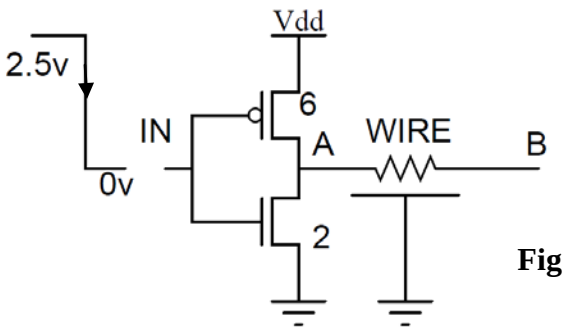

Fig 2

a) Determine the source impedance **Zs** at the source end of wire

b) Draw schematic of a driver at destination end to get destination impedance Z_T = 1 kΩ

c) Sketch and label lattice diagram to show voltage amplitude at source and destination nodes as destination voltage gradually reaches its final value of *Vin* = 2.1 V. Hence, calculate signal propagation delay from A to B. Also, sketch and label the waveform of destination voltage w. r. t time.

d) Determine the signal propagation delay from A to B if driver at destination end is a CMOS inverter designed with Wp:Wn=3:1

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Q3. For radix 2 KOGG STONE (KS) PG diagram shown in Fig. 3-

Redraw a neat labeled radix 3 KS PG diagram. Hence compute parameters l, f, t

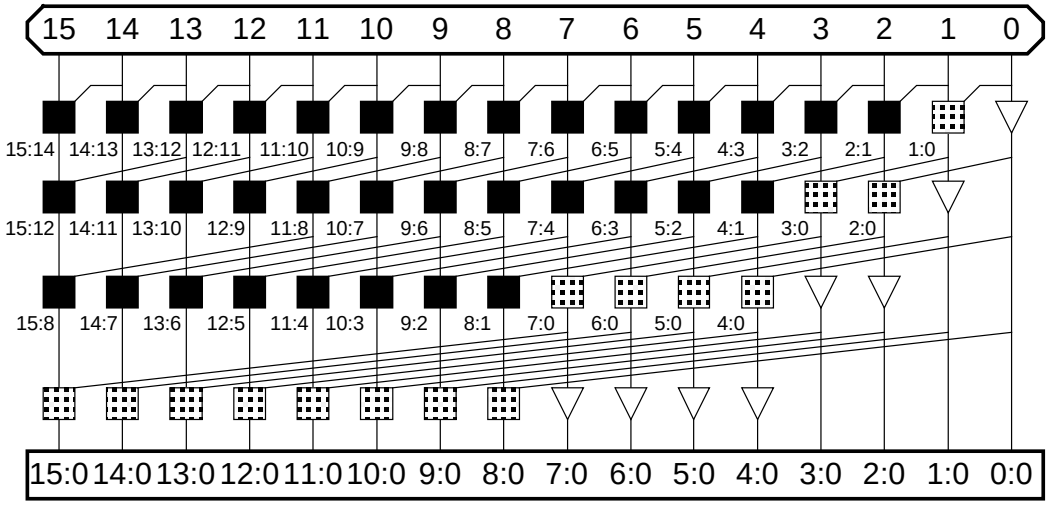

Fig 3

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Q4. For circuit of Fig 4---

a) Explain the operation of this circuit as signal propagates from D to Q. Write neatly in steps. Can we use all transistors minimum size in this circuit?

b) Explain the purpose of signal at node **c**, and **d.**

c) Write the expression of setup time, hold time and clock to Q delay, clock load, and clock time period (low phase and high phase both)

d) Discuss the sensitivity of this circuit to (1-1) and (0-0) clock overlap. If yes, how will you overcome the clock overlap problem?

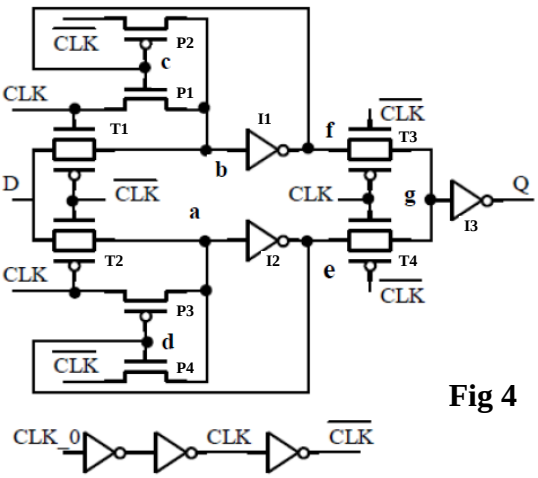

Fig 4

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Q5. A 70 cm long wire length in clock path has width of the wire as 1um, *capacitance per unit length* $\boldsymbol{c}$ = 110 x 10^{-18} F/um, $\boldsymbol{r}$ = 0.075 Ω /um, $\mathbf{Z_o}$= 60 Ω.

a) Determine the signal propagation delay through the wire length.

b) Determine maximum length of the wire, and corresponding maximum rise (or fall) time of the input signal for which we should consider transmission line effects in wire delay calculation.

c) In part (a), CMOS inverters are placed at regular intervals across the entire wire length. Determine propagation delay $\mathbf{t_p}$ of CMOS inverter. Also, determine the minimum critical length L_{crit} of the interconnect wire segment (between two inverters) where $(RC)_{wire}$ delays are dominant. Take that CMOS inverter has (t_{phl}=t_{plh}) .Hence re-calculate the total signal propagation delay through the wire with CMOS inverter

d) Explain the difference in the design of chain of CMOS inverters to drive a heavy capacitive load and chain of inverter to distribute a clock signal in clock distribution network

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