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I SEMESTER, 2016-2017

MIDSEM TEST CLOSED BOOK (1 Oct. 2016)

MEL G623 ADVANCED VLSI DESIGN

TIME-90 MTS. **MAX. MARKS=25**

NOTE: Answers should be clear, concise and legible. Specify your assumptions clearly. Do all parts of same question together. Diagrams should be neat. NO MARKS for unnecessary theoretical explanation. Justify your answers

Take $u_n = 2\,u_p$, *ginv=1, pinv=1,* Vdd=3.3 V, |Vtn|= |Vtp|= 0.7V, $W_{min}=L_{min}$= 180 nm , Gate capacitance: C_{ox}(NMOS) = C_{ox}(PMOS) = 6 fF/μm^2, 180nm technology for all questions, velocity of electromagnetic wave= 15cm/ ns

Q1. For the fig 1, an external clock (Clk_{in}) is routed to the center of the chip, where the first buffer is located. The chip itself is divided into four quadrants. The buffered clock is distributed to each of the quadrants, where a second buffer stage is inserted, which drives the final loads (as annotated on the Fig 1) as a function of the unit capacitance *Cu*, which is the input capacitance of the first buffer, and is equal to the input capacitance of a minimum-sized inverter (This means that the first stage of the first buffer MUST be a minimum-sized inverter)

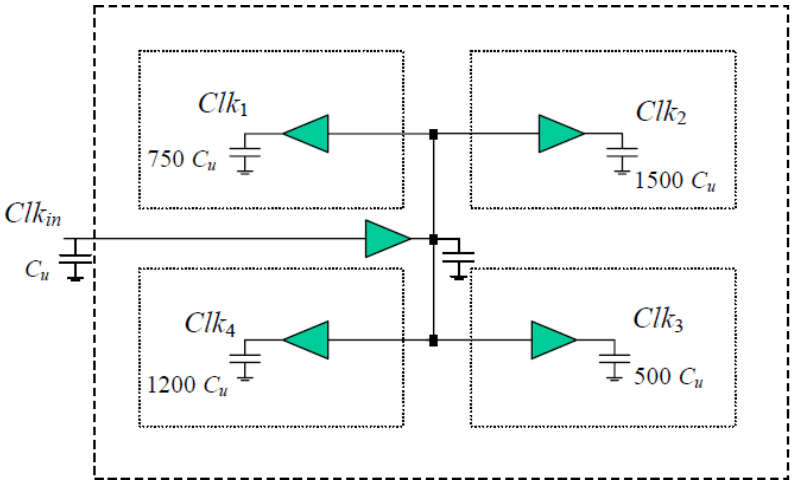

Fig 1

Each dashed "buffer" box represents a chain of inverters. Ignore wiring capacitances. For 180 nm technology, take τ= 50ps, Vdd=3.3 V, |Vtn|= |Vtp|= 0.7V

a) Design the buffer '**Clk_1**', and '**Clk_2**' (number of stages, device sizes) with minimum possible propagation delay from *Clkin* such that following specifications are met:
   - The number of inversions between the input clock signal and the load MUST be even
   - The clock skew between the clock signals ($Clk_1 - Clk_2$) is ≤. |150ps|. Assume ideal input clock

b) Determine the optimum number of stages that should be chosen to design buffer for clk3 to meet the skew constraint.

c) Design a low power low swing clock driver which can replace inverter (in chain of inverters) in (a) part

10

Q2. Answer the following in brief--

a) Describe the difference between a data flip-flop and synchronizer. Can a data flip flop be converted into a synchronizer? If yes, how?

b) Sketch and label the wave forms (clk, D, Q) to represent the setup and hold time for register and latch separately.

c) Describe the difference between edge triggered design and event triggered asynchronous design. Which protocol is edge triggered?

6

Q3. For fig 2, assume latch capacitive load identical to skewed inverter

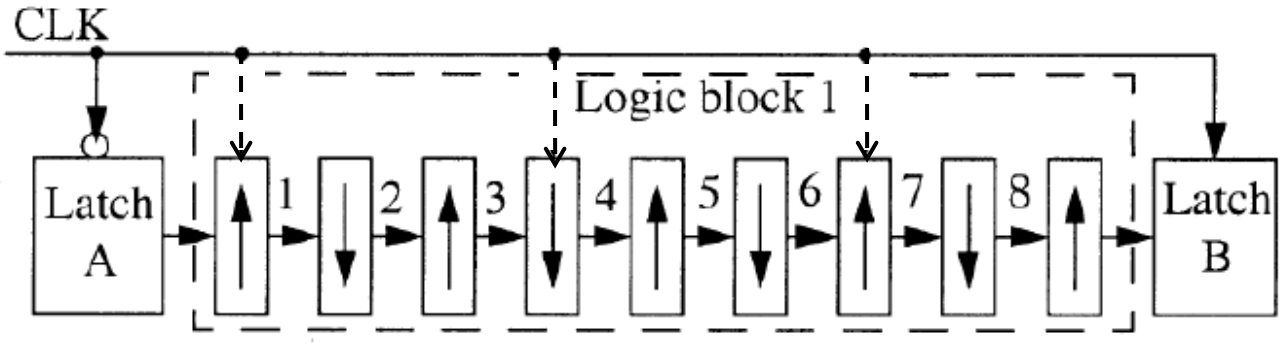

Fig 2

Ignoring clk signal (dashed arrow)

a) Design (schematic) of a chain of skewed inverters favouring up/ down transition as shown in fig 2

b) Estimate the delay for rising output

c) Estimate the power consumption per clock cycle for the above circuit. Ignore wire and parasitic capacitances. Take gate capacitance as given in instructions

Considering clk signal (dashed arrow)

d) Draw the circuit only of a chain of skewed inverters favouring up/ down transition in part (a)

9
